Rui Miguel Lopes Borrego

Licenciado em Ciências da Engenharia Eletrotécnica e de Computadores

A Low-Voltage RF-CMOS Receiver Front-End for a Wireless Fall Detection Microsystem

Dissertação para obtenção do Grau de Mestre em Engenharia Eletrotécnica e de Computadores, pela Universidade Nova de Ciências e Tecnologia

Orientador: Prof.Doutor João Pedro Oliveira, FCT-UNL

Presidente: Prof. Doutor(a) Luis Brito Palma
Arguente(s): Prof. Doutor(a) Luis Bica Oliveira

FACULDADE DE CIÊNCIAS E TECNOLOGIA
UNIVERSIDADE NOVA DE LISBOA

Dezembro 2013

A Low-Voltage RF-CMOS Receiver Front-End for a Wireless Fall Detection Microsystem

I dedicate this project to my entire family, notably to my mother Maria Câpelo, to my father José Borrego, to my brother Ricardo Borrego, to his wife Tânia Fonseca, to my cousins Paulo Almeida and Fernando Almeida, to my uncles Fernando Serrano and Cacilda Serrano, to my grandmother and grandfather Maria Chora, Gracinda Borrego, Amadeu Câpelo, Manuel João Borrego, to my future wife and sons and to my lovely godson Gabriel Fonseca.

Acknowledgments

I would specific like to thank to my leader professor João Pedro Oliveira for all the support and advices given during this year. I would also like to thank to others professors such as: Adolfo Steiger, João Goes, Luis Oliveira, Nuno Paulino, Helena Fino, Rui Tavares, Fernando Coito, Michael Figueiredo, Rui Diniz, Mário Macedo and Pedro Montezuma that had a big role in my growing as electrical and electronic engineering student in several subjects.

I would like to thank to my department of electrical and electronic engineering and to the university Nova de Lisboa due to the good conditions to work. I also would like to thank to my work colleagues Nuno Diniz, Ricardo Silva, Francisco Marques, Francisco Esteves, Patrick Boura, Ricardo Lampreia, Ricardo Ferreira, Pedro Pinto, Pedro Canto, Gonçalo Barros, Debs Tavares, Fernando Teixeira, António Furtado, José Baleia, Frederico Braga, Bruno Pereira, Igor Pereira, Tiago Cabral, David Palma and André Lourenço for the support and help since, i started the course.

Related with the thesis, i would also like to thank to my colleagues Fábio Querido, Hugo Serra, Fábio Passos, Diogo Inácio, Pedro Leitão, David Amoedo and Nuno Pereira for all the support and help given during this year.

Universidade Nova de Lisboa

Resumo

Faculdade de Ciências e Tecnologia

Departamento de Engenharia Electrotécnica e de Computadores

Mestrado Integrado em Engenharia Electrotécnica e de Computadores

por

Nesta tese um conjunto, Amplificador de baixo ruído-misturador é apresentado. O Amplificador de baixo ruido é composto por um "common-gate" , por um "common-source" e por um "buffer" com o objetivo de que o circuito funcione em "single-end". O Misturador é composto por uma estrutura típica "common-gate". O desenvolvimento deste bloco teve como propósito a implementação do mesmo, num sistema de deteção de quedas para doentes que fosse capaz de monitorizar o estado e comportamento do paciente remotamente por um unidade hospitalar. O desenvolvimento deste circuito não teve só como objetivo a prevenção de quedas mas também, o contributo para o desenvolvimento da Medicina, assim como para a mais diversa investigação em centros de pesquiza. Foi projetado para cobrir as bandas de frequência ISM e WMTS, desde os 400 até aos 900MHz e para operar a reduzida tensão compreendida numa gama de 0.6 a 1.2 V.O sistema foi totalmente implementado com MOSFETs sem uso de elementos reativos utilizando a tecnologia UMC CMOS de 130 nm. Técnicas simples são utilizadas no desenho e otimização tendo como objetivo a reduzida tensão e o baixo consumo. O circuito apresenta um consumo total de 11.5 mW, extraídos de uma fonte de 1.2 V e um consumo total de 3.5 mW extraídos de uma fonte de 0.6 V.

Universidade Nova de Lisboa

Abstract

Faculdade de Ciências e Tecnologia

Departamento de Engenharia Electrotécnica e de Computadores

Mestrado Integrado em Engenharia Electrotécnica e de Computadores

by

In this thesis a Low Noise Amplifier-Mixer, the LM, is presented. In the Low Noise Amplifier a common-gate, a common-source and a buffer were used and the last one with the target to work in single-end configuration. A typical structure common-gate was used in the Mixer. The development of this structure had as goal, the implementation of a circuit capable to be used in a fall detection system for disable patients, monitoring the state and behavior remotely by an hospital. The conception of this circuit did not have only the objective, the prevention of falls, but also the contribute for the Medicine enrichment, as well as the research in several institutions. It was developed to cover ISM and WMTS frequency bands since 400 to 900MHz and to operate at low voltage in a range values between 0.6 and 1.2 V. The system was totally implemented with MOSFETs without reactive elements using the UMC CMOS 130 nm technology. Some techniques are used in design and optimizing with the target of low voltage and low consumption. The circuit present a total consumption of 11.5 mW extracted from a supply voltage of 1.2 V and a consumption of 3.5 mW extracted from a supply voltage of 0.6 V.

Content

Copyright III
Acknowledgments VII
Abstract XI
List of Figures XV
List of Tables XVII
Abbreviations XIX
1 Introduction 1
1.1 Background and Motivation 2
1.2 Thesis Organization 2
1.3 Main Contributions 3
2 Receiver Architectures for Fall Detection Microsystem 5
2.1 Fall Detection Microsystem Structure 5
2.2 Receiver Architectures 7
2.2.1 Heterodyne Receiver 8
2.2.2 Homodyne Receiver 8
2.2.3 Low IF Receivers 9
2.3 Low Noise Amplifiers 11
2.3.1 Principal LNA Points of study 11
Stability 11
S-Parameters 12
Power Gain and Voltage Gain 12
Noise Factor 13
2.4 Mixers 13
2.4.1 Principal Mixers Points of study 13
Conversion Gain 13
Noise Factor 15
Passive Mixer 17
Active Mixer 18
3 Low Voltage and Wideband Techniques for LNA and Mixer 19
3.1 Mosfet Operation under Low Voltage Conditions 19
3.2 Wideband Configuration for Amplifiers 20
3.3 Typical Balun LNA 22
3.4 Proposed Balun LNA 23
3.5 Single end Mixer design 27
4 Proposed Balun LNA and Mixer Simulation 29
4.1 LNA Simulations 29
4.2 Mixer Simulations 41
5 Design and Simulations of a Combined LNA and Mixer 43
6 Conclusion and Future Work 59
Bibliography 63
Appendix A CMOS Basic Information 67
Appendix B CMOS Published Paper 85

List of Figures

Figure 1-Block Diagram. 6
Figure 2-Transceiver. 6
Figure 3-Heterodyne Receiver. 8
Figure 4-Homodyne Receiver. 9
Figure 5-Low IF Receiver. 9
Figure 6-Low IF Receiver. 10
Figure 7-S-Parameters 12
Figure 8-Network. 13
Figure 9-Network. 14
Figure 10-Conversion Gain. 16
Figure 11-Noise Factor. 16
Figure 12-Passive Mixer 17
Figure 13-Active Mixer 1ºArquitecture. 18
Figure 14-Active Mixer 2ªArquitecture. 18
Figure 15-DTMOS Configuration. 19
Figure 16-Vth in function of Vbs. 21
Figure 17-Resistor Replaced by Transistor. 21
Figure 18-Balun LNA. 22
Figure 19-Proposed LNA. 23
Figure 20-First Stage Small-Signals. 23
Figure 21-Buffer Output. 25
Figure 22-Proposed Mixer. 27
Figure 23-Transient Simulations at 1.2 V. 31
Figure 24-Phase Simulation at 1.2 V. 31
Figure 25-Gain Simulations at 1.2 V. 32
Figure 26-Noise Factor Simulations at 1.2 V. 32
Figure 27-S11 Parameter Simulations at 1.2 V. 33
Figure 28-Gain Simulations at 0.6 V. 35
Figure 29-Noise Factor Simulations at 0.6 V. 35
Figure 30-S11 Parameter Simulations at 0.6 V. 36
Figure 31-IIP3 Simulations. 36
Figure 32-TT Simulations at 0.6 V. 37
Figure 33-FF Simulations at 0.6 V 37
Figure 34-SS Simulations at 0.6 V. 38
Figure 35-Simulations with and without DTMOS at 0.6 V. 38
Figure 36-Simulations with and without DTMOS at 0.6 V. 39
Figure 37-Gain Simulations at 1.2 V. 41
Figure 38-Noise Factor Simulations at 1.2 V. 41
Figure 39-LNA+MIXER. 43
Figure 40-Gain Simulations at 1.2 V. 46
Figure 41-Noise Factor Simulations at 1.2 V. 46
Figure 42-Gain Simulations at 0.8 V. 49
Figure 43-Noise Figure Simulations at 0.8 V. 49
Figure 44-Gain Simulations at 0.6 V. 52
Figure 45-Noise Factor Simulations at 0.6 V. 52
Figure 46-TT Simulations at 1.2 V. 53
Figure 47-FF Simulations at 1.2 V. 53
Figure 48-SS Simulations 1.2 V. 54
Figure 49- TT Simulations at 0.8 V. 54
Figure 50-SS Simulations at 0.8 V. 55
Figure 51-TT Simulations at 0.6 V. 55
Figure 52-Gain in Function of Vdd. 57
Figure 53-Noise Factor in function of Vdd. 58
Figure 54-PDC in function of Vdd. 58
Figure 55-NMOS and PMOS Transistors. 68
Figure 56-NMOS and PMOS Transistors. 68

Figure 57-Modes of Operation. 69
Figure 58-Modes of Operation. 70
Figure 59-Flicker Noise. 73
Figure 60-Flicker Noise. 74
Figure 61-1 dB Gain Compression Point. 75
Figure 62-Ampop. 76
Figure 63-Input Frequencies. 77
Figure 64-Output Frequencies. 77
Figure 65-Common Source Circuit. 78
Figure 66-Common Source Small Signals. 78
Figure 67-Common Gate Circuit. 80
Figure 68-Common Gate Small Signals. 80
Figure 69-Common Drain Circuit. 82
Figure 70.Common Drain Small Signals. 82

List of Tables

Table 1-Transistors gm values. 26
Table 2-Transistors size at 1.2 V. 30
Table 3-Results at 1.2 V. 33
Table 4-Transistors size at 0.6 V. 34
Table 5-DC Operating Points at 0.6 V. 34
Table 6-Results at 0.6 V. 39
Table 7-Models Transistors Results. 39
Table 8-Comparison between DTMOS and MOS. 40
Table 9-Transistors size at 1.2 V. 42
Table 10-DC Operating Points at 1.2 V. 42
Table 11-Transistors size at 1.2 V. 44
Table 12-DC Operating Points at 1.2 V. 45
Table 13-Transistors size at 0.8 V. 47
Table 14-DC Operating Points at 0.8 V. 48
Table 15-Transistors size at 0.6 V. 50
Table 16-DC Operating Points at 0.6 V. 51
Table 17-Results at 10MHz. 56
Table 18-Models Transistors Results at 1.2 V. 56
Table 19-Models Transistors Results at 0.8 V. 56
Table 20-Models Transistors Results at 0.6 V. 56
Table 21- Balun LNA VS Proposed LNA. 60
Table 22-Performance Proposed LNA VS Others 60
Table 23-Theoretical and Pratical results 61
Table 24-Configuration characteristics. 83

Abbreviations

ADC	**A**nalog to **D**igital **C**onverter
AC	**A**lternating **C**urrent
CD	**C**ommon **D**rain
CG	**C**ommon **G**ate
CMOS	**C**omplementary **M**etal-**O**xide-**S**emiconductor
CS	**C**ommon **S**ource
DC	**D**irect **C**urrent
IF	**I**ntermediate **F**requency
ISM	**I**ndustrial **S**cientific and **M**edical
IIP	**I**nput Referred **I**nterception **P**oint
GPS	**G**lobal **P**osition **S**ystem
LV	**L**ow **V**oltage
LNA	**L**ow **N**oise **A**mplifier
LO	**L**ocal **O**scillator
LM	**L**NA **M**ixer
NF	**N**oise **F**actor
NMOS	**N**channel **M**etal-**O**xide-**S**emiconductor
PA	**P**ower **A**mplifier
PLL	**P**hase **L**ocked **L**oop
PMOS	**P**channel **M**etal-**O**xide-**S**emiconductor
RF	**R**adio **F**requency
WMTS	**W**ireless **M**edical **T**elemetry **S**ervice

Chapter 1

Introduction

1.1 Background and Motivation

Since that technology and electronic devices associated, started to have an heavy impact in society, several instances and companies had the necessity to improve and develop others systems more robust and capable to compete in many fronts and in many economic markets. Many sectors of society such as medicine, video games industry, telecommunications services and areas related with microchips and computers, were crucial for the growing of electronic, as well as all the techniques used to support that maturity.

Nowadays, the low voltage and low consumption electronic systems are the required to the preferential demand in industry and this reality has more and more impact in all firms, workers and consumers around the world. Several research has been done in universities and it is thought, which that study indirectly has been modified and could modifier further the engine of evolution. The goal of this thesis is develop a receiver constituted by two crucial blocks that could be used in a fall detection system, one of them is the Low Noise Amplifier and the other is the Mixer, these two components have to be capable to work in a voltage range between 0.6 and 1.2 V and in a bandwidth range between 450 and 900 MHz.

They have to have the capacity to labor in unpleasant weather conditions that could be sense in Africa or North Europe for example. The importance of them are known, every receptor or transceiver has one. Shortly for easy understanding, the LNA has the function to receive information from another receiver for example and to guarantee the quality of that information, which is translated in a signal, there are two parameters, which them values have to be good, the gain and the noise factor and these parameters are the reason why this block is the most important in a receiver topology. The Mixer allows that the circuit internally could work with lower frequencies instead of the traditional RF such as 2.4 or 5 GHz which are not compatible.

To achieve the low voltage and low consumption objective, are used some techniques such as, the DTMOS, the voltage controllers and the resistor replacing by a transistor in triode region, which will be explained in detail posteriorly, but at this moment it is crucial to understand that these solutions are the base and without them the success of this work will not be possible.

When a kind of this project is done, there are several motivations involved. The first is directly related with the research and the fact that such circuit could be improved and studied by another student or professor in the future and make possible the layout and possibly a contact with a physic circuit, which will be enriching to the knowledge. The development of a system, which could be used to cultivate the medicine market through many devices that use receivers and indirectly help disable people or at least contribute to that thinking is rewarding.

It is known that more and more, it is difficult to follow the technology, and such that is innovator in the present passed some months will not be, because the exigency of firms to gather better products that could be cheaper and economic, therefore contribute for that competition with new ideas or simply trying to improve them, should be part of each engineering student.

1.2 Thesis Organization

This thesis is organized with more six chapters as follows:

Chapter 2 – Receiver Architectures for fall Detection Microsystem

In this chapter are done descriptions of the principal receiver's topologies that can be used in fall detection microsystems, as well as for the principal receiver blocks such as: LNA and Mixer. Cases of study such as, flicker noise, gain conversion, S-parameters and stability also are reported and discussed.

Chapter 3 - Low Voltage and Wideband Techniques for LNA and Mixer

In this chapter it is explained the three important techniques used in the circuit: The DTMOS, the voltage controller and the use of a transistor in triode region instead of a simple resistor. It is also explained mathematically why the difference and the advantages, when they are used and it is done also a mathematic study for the LNA and Mixer proposed.

Chapter 4 – Proposed Balun LNA and Mixer Simulations

In this chapter are showed figures with simulations done for the gain, noise factor and IIP3, as well as tables with the sizing of each transistor and DC operating points at different supply voltage values. PVT simulations are also done.

Chapter 5 – Design and Simulations of a Combined LNA and Mixer

In this chapter, it is showed the total circuit and again are showed figures with simulations done for the gain, the noise factor as well as PVT simulations. Are showed in tables also the sizing for each transistor and DC operating points at different supply voltage values.

Chapter 6 - Conclusions and futures works

In this chapter, it is discussed the main conclusions of this thesis and the future works, which could be done by the author in PhD or by some another student or professor interested. It is also referred the advantages and disadvantages of this LM.

1.3 Main Contributions

This thesis contributed for the scientific community with one paper presented in 2013 MIXDES conference in Poland. This was developed directly related with the main theme of this work entitled "A 2.3-dB NF CMOS Low Voltage LNA Optimized for Medical Applications at 600MHz". Others Contributions can be done in future works with the possibility of make a full receiver in PhD.

Chapter 2

Receiver Architectures for Fall Detection Microsystem

The main objective of this chapter, is to offer some important knowledge of several receivers that are used in these days, which can be used in fall detection systems. Their principal characteristics, some points of view, advantages and disadvantages, which are very important when, it is necessary to choose a good topology to work in RF area.

It will be presented a brief theoretical overview related with the most important aspects of these architectures that can be central to the understanding of this thesis for the experts or no in the area in study. Since, the objective of this thesis is design a low voltage receiver circuit in CMOS technology that includes several RF front end blocks such as a LNA and Mixer, it will be given a detailed explanation of each part.

2.1 Fall Detection Microsystem Structure

It is crucial for the global understanding, the description and visualization of the principal blocks that are used in this kind of structure. Mixer and LNA can be the most important circuits working in a transceiver, but obviously there are others systems such as, sensors, buffers and filters, which have a fundamental role enabling the communication and the collecting of vital signals.

It was thought to use three important sensors, an accelerometer to detect the x, y and z coordinates of each person, in this case the coordinates are used to know if the patient is in lying, sitting position as well as, if there was any outburst movement for example. A temperature and pulse detector are also thought with the objective to measure the vital condition and rapidly alert an hospital or a doctor.

In Figure 1 and Figure 2, it is verified an example how a block diagram could be and it can be divided in two parts. The first one is related with the all external configuration responsible for the signal collecting and the second one responsible for the treatment information.

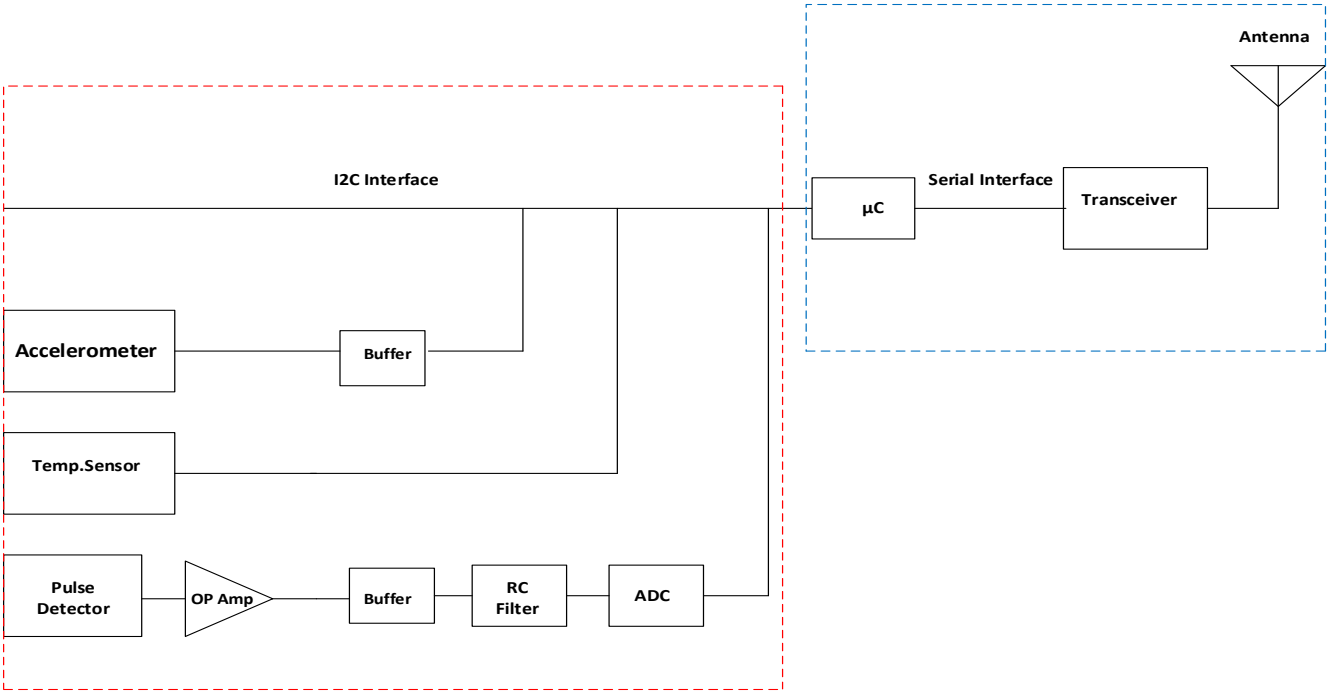


Figure 1-Block Diagram.

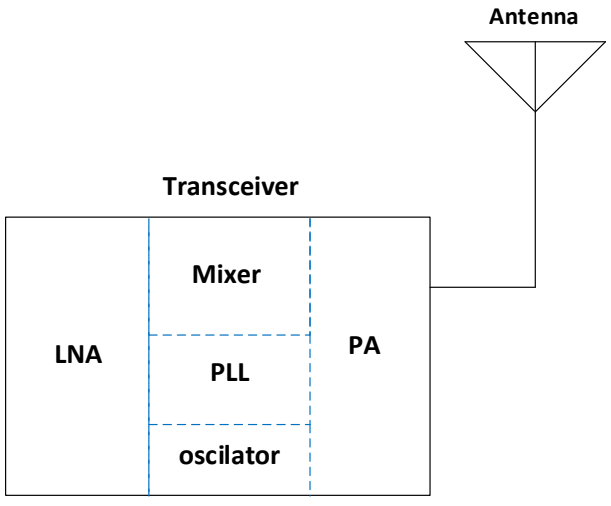


Figure 2-Transceiver.

These configurations only show the main blocks presented in the system, obviously that exits several techniques and circuits surrounding, which support the LNA and the Mixer. In this case it is possible to note five components: LNA, Mixer, Pll, oscillator and the power amplifier. In general for global understanding the LNA has the objective to capture de signal, that signal it is treated and modulated by the three blocks in the centre and it is sent to other antenna through power amplifier.

2.2 Receiver Architectures

In several equipment's and devices, the RF technology has a massive impact and for that reality receivers are fundamental. Radios, cellphones, GPS, routers or fall detection systems, both use this technology to make the data transference between them correctly. It can be possible to work with many frequencies in many distinct applications such as ISM, WMTS, GSM, UMTS and more recently LTE. The receivers have not only a big role in electronic but, also in telecommunications.

Speaking more specifically about this topic, higher frequencies are used because higher bandwidths are required, therefore it is difficult to design and project a consistent receiver and further when LV is necessary. Also when a receiver is developed, exist other issues that can complicate his structure such as the reception signal, which can be bad due to the noise and distortion caused by exterior elements, other problems such as weak input signals are also a big deal when these devices are design. It could be different to develop a receiver to communicate with other receiver at the same frequency instead of develop a receiver to communicate with a sensor for example that works with lower frequencies.

Receiver's devices are compound by many blocks as it is known but, also it is known that the most important block is the LNA, therefore it is central to obtain a good gain and NF, but the massive importance of this block in receiver performance, will be explained with more detail in other part of this chapter. By now will be explained some commonly used topologies with different targets.

2.2.1 Heterodyne Receiver

This type of receiver showed in Figure 3[1], is one of the most used receiver architectures in wireless communications systems. The down conversion can be divided in two steps, in the first one the input signal is translated to the IF band which is fixed. The first block of the system has the duty to select the target band and then the input RF signal is amplified by a LNA and translated.

This operation is done by a mixer and create two replicas of the input signal. After the all unwanted image signals be cleared, the RF signal is again down-converted to the baseband. The mixer output is again filtered by a channel selection filter and posteriorly the signal can be down-converted to baseband, but for that work is necessary the perfect LO quadrature signals (I/Q balance). Finally with the signal on the band base there is only a low pass filter and an ADC that frames the signal to be demodulated in the digital domain [1].

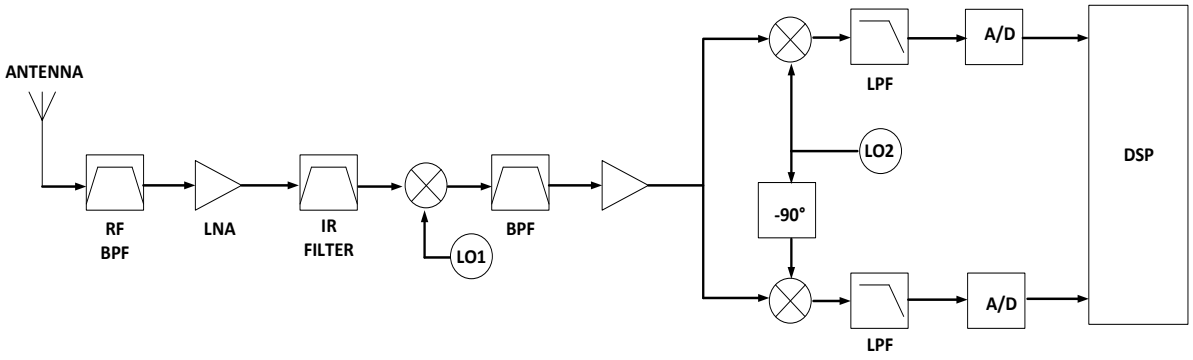


Figure 3-Heterodyne Receiver.

2.2.2 Homodyne Receiver

This type of receiver showed in Figure 4 [1], is simpler than the heterodyne architecture and allows the possibility of complete integration if it not necessary high quality filters. Due to the RF signal be directly translated to the baseband, the receiver is affected by flicker noise and because this, the system doesn't assure perfect isolation between their blocks and oscillator leakage can occur. The leakage entails problems related with the appearance of undesired DC

components that may result in receiving process corruption and it is due to capacitive coupling and ground problems [1, 3].

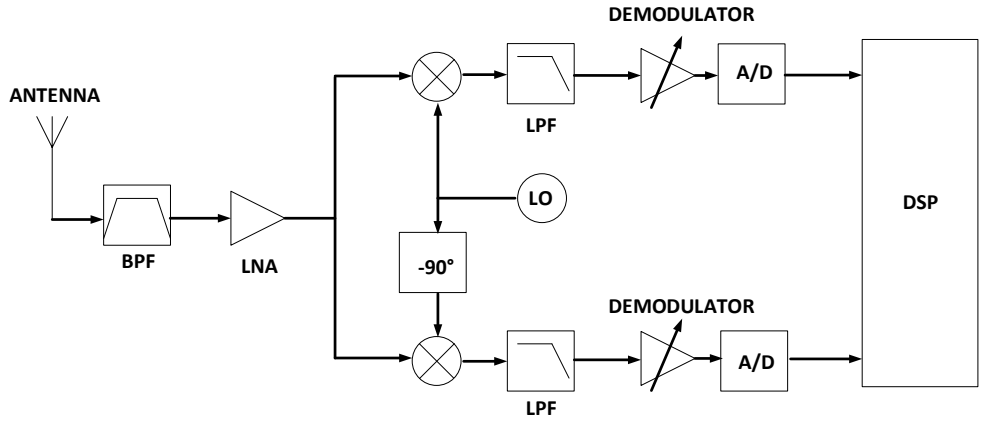


Figure 4-Homodyne Receiver.

2.2.3 Low IF Receivers

This type of receiver showed in Figure 5 [13] and Figure 6 [13] is a combination between the heterodyne and the homodyne architectures, is used a mixed approach which consists in using the homodyne receiver but instead of doing a direct conversion to base band, the signal is shifted to a low intermediate frequency, so the base band problems are avoided, but it is still mandatory to overcome the image problem. For solve this issue can be used two different types of techniques: the Hartley and Weaver architectures. The concept is to process the signal after the low pass filter and combine both outputs into a single one, with this action the image is suppressed through its negative replica [2, 3].

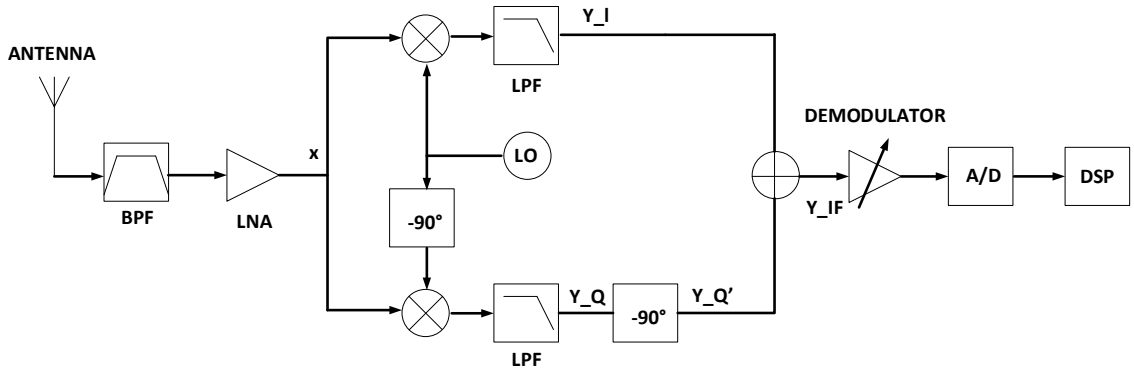


Figure 5-Low IF Receiver.

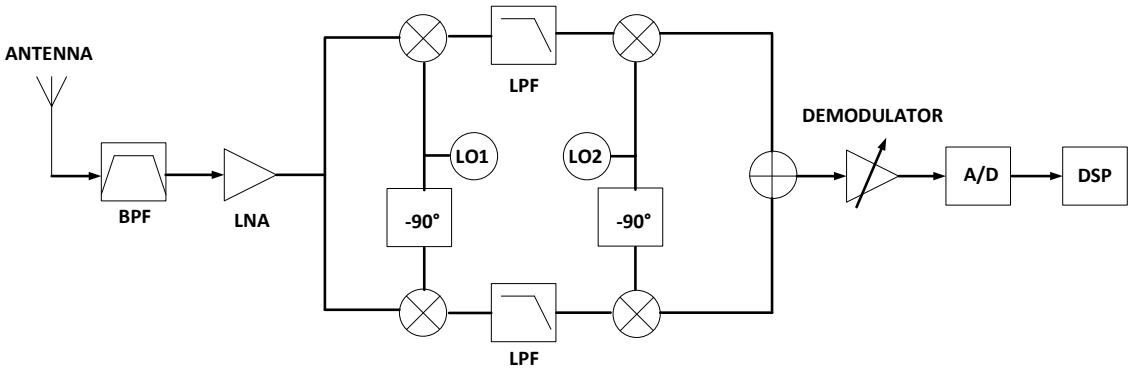


Figure 6-Low IF Receiver.

It is important to note that these topologies have also to work with low voltage supply values and doing a short framework with the theme of this thesis, it is possible to give an example that it is showed in this paper [13], how this circuit can operate when some techniques are applied.

.

2.3 Low Noise Amplifiers

Low Noise Amplifiers are the most important devices of a receiver, and without start with Mathematics equations in this first introduction, it is known that in general them main goal is related with the circuit compensation, due to the losses of the others components such as Mixers that does not have practically gain in some topologies when the Noise Figure is high, thus to compensate these situation LNA's are critical. To guarantee the good operation of a receiver, it is mandatory the LNA could be provided with high gain and low noise factor, but to achieve that target sometimes is necessary to use some techniques.

2.3.1 Principal LNA Points of study

Some points that are important to discuss in this chapter such as:

Stability

The first point that has to be considered, before start to develop a LNA is the stability. This term is used to verify the circuit stability and is calculated through S-Parameters as it is possible to see verifying the equation 2 [1].

$$K = \frac{1 - |S_{11}|^2 - |S_{22}|^2 + |\Delta|^2}{2|S_{12} * S_{21}|} \text{ , } \Delta = S_{11}S_{12} - S_{12}S_{21} \quad \textbf{(2)}$$

If K > 1 and $|\Delta| < 1$ the LNA is stable, this notion is more used to bipolar transistors, but is also noted for the CMOS transistors when for example some simulations are done in software Cadence.

S-Parameters

To analyze correctly the performance of a LNA, it is important to study some parameters defined by S_{21}, S_{12}, S_{11} and S_{22}. S_{21} represents the forward voltage gain, S_{12} the reverse gain voltage, S_{11} the input port voltage reflection coefficient and S_{22} the output port voltage reflection coefficient. In the Figure 7 [1] is shown a good example, how these parameters are represented in a circuit. Usually when a LNA is developed and simulated normally, it is possible to assume some values to verified if corresponds a decent circuit or not [1]. In other words for the expert and

common lector, S_{21} is related with the capacity of a LNA to amplify the signal in good conditions, so how much bigger is this parameter, better the performance. S_{12} is the reverse gain and it is a kind of response in relation to $S_{21,}$ therefore it is required that this parameter value could be very small like -30 or -40 db. The parameters S_{11} and S_{22} are also important in this study and their values represent the capacity of input and output matching of a LNA with a load impedance with 50 Ω approximately.

When it is referred about only LNA circuit, the output is relevant to obtain good simulations, but if it is spoken about the global circuit where is necessary to connect this device to another device by a transistor, does not make sense to refer about it [1].

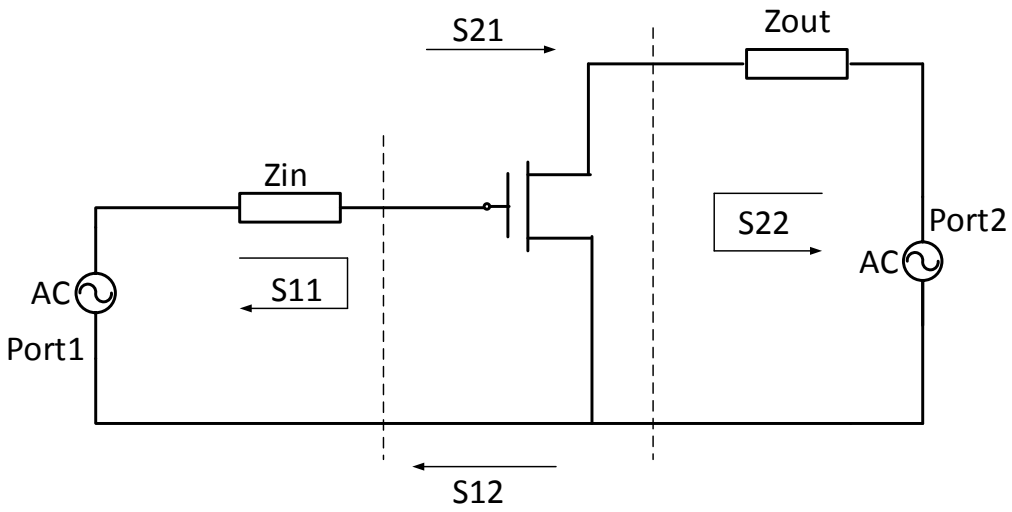


Figure 7-S-Parameters

For example, a LNA working at 1.2 Voltage supply with 16 db of S_{21} and -12db of S_{11} and S_{22} is acceptable in general, depending the application required certainly.

Power Gain and Voltage Gain

This point is important, to understand the differences between several simulations that are possible to do in Cadence, for example if it is tried to get the gain of the LNA by psp or pss simulation, the result could be different, if it is tried to get the gain by transient simulation, because S-parameters give the power gain and the transient response give the voltage gain and these values can be different, if for example the circuit does not be input/output matched correctly [1].

When it is necessary to simulate any circuit where is crucial to study his real gain, specifically in this case, circuits like LNA, the first simulation, which is crucial to obtain the first impression of the circuit performance is transient/ac response, because with this simulation there is no doubts. These two types of gain can be given by the equation 2.1 [1] and equation 2.11 [1]:

$$Power\ Gain = 10\log\left(\frac{Pout}{Pin}\right) \quad \textbf{(2.1)}$$

$$Voltage\ Gain = 20\log\left(\frac{Vout}{Vin}\right) \quad \textbf{(2.11)}$$

Noise Factor

The Noise Factor is also, one of the most crucial aspects to analyze the quality of a LNA. How much lower is his NF, lower will be the final NF global circuit, so it is extremely important to optimize him. Usually, it is not easy to define the best value for a circuit because this value can depends the application required, but for the majority of cases and low voltage too, a noise factor lower than 4 dB is acceptable.

Speaking generally about this noise it is known that it is related with thermal noise, therefore for the experts, the noise factor is defined as the ratio of the total available noise power at the output of the amplifier to the available noise power at output due to
thermal noise from the input termination resistance at T=290K, this ratio can be expressed by equation 2.12 [1].

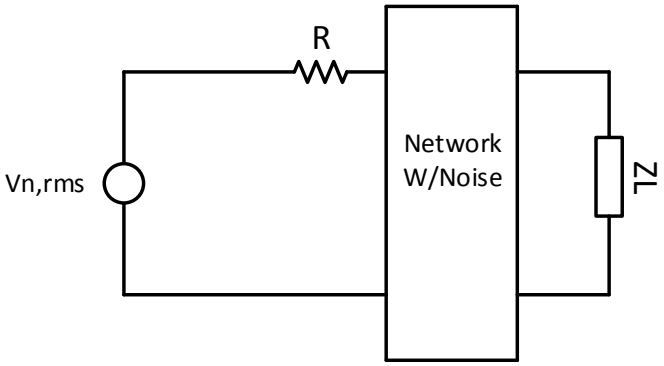


Figure 8-Network.

$$F = \frac{P_{NO}}{P_{NI} * G_A} = \frac{P_{NO}}{P_{NI} * \frac{P_{SO}}{P_{SI}}} = \frac{\frac{P_{SI}}{P_{NI}}}{\frac{P_{SO}}{P_{NO}}} = \frac{SNR_i}{SNR_o} \quad \textbf{(2.12)}$$

where the P_{NO} represents the available noise power at the output, P_{NI} the available noise power at the input, P_{SI} the available signal power at the input, P_{SO} the available signal at the output. In the beginning of this chapter it was referred that LNA was the most important block in a receiver, and now it will be show why. If it looked to the equation 2.13 [1], it is easy to understand that the gain of LNA is present in every block of the receiver, therefore it is extremely important to have a good gain in the first block to compensate the others [1]. A basic configuration can be shown in Figure 8 [1] and Figure 11 [1].

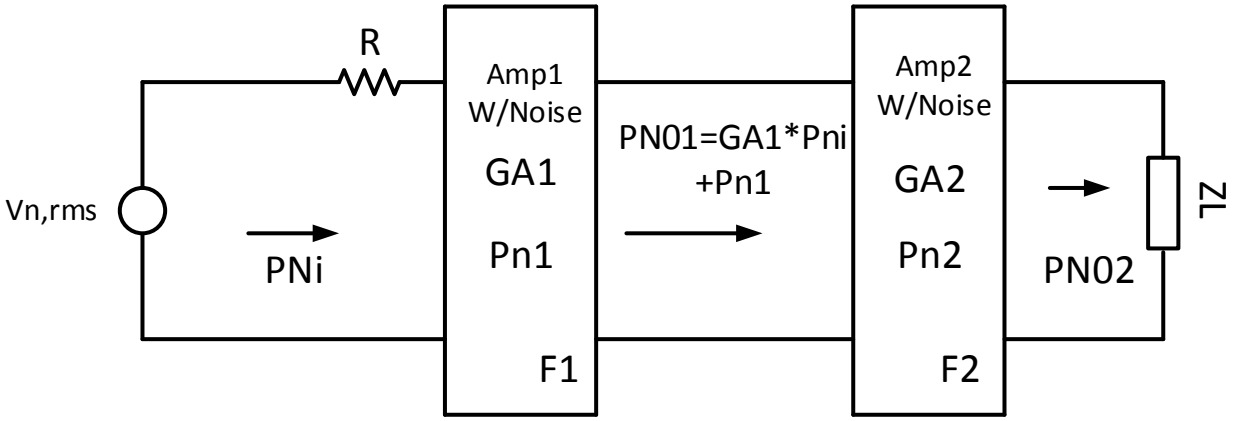


Figure 9-Network.

$$F = \frac{P_{N02}}{P_{NOi} * G_{A2} * G_{A2}} = \frac{G_{A2} * (P_{Ni} * G_{A1} + P_{n1}) + P_{n2}}{P_{Ni} * G_{A1} * G_{A2}} = F1 + \frac{F2 - 1}{G_{A1}}$$

$$F = F1 + \frac{F2 - 1}{G_{A1}} + \frac{F3 - 1}{G_{A1} * G_{A2}} + \cdots \quad \textbf{(2.13)}$$

2.4 Mixers

The following block that has a big role in a receiver, it is the Mixer and his name state everything, because the main objective, it is mixed two sinusoidal signals, the signal that has as source, the LNA and the signal that has as source the oscillator. This device is crucial due to the fact to enable the receiver works with another frequency, in other words with the internal work frequency, so if it is required internally work with for example 10MHz, it is necessary to have a LNA that works at 600MHz and a oscillator that works at 610MHz.Usually, a typical Mixer does not have gain or even sometimes the gain is negative because his target is not to give gain to the system but make the mix correctly.

In general applications related with electronic and telecommunications devices, a gain with 2 or 4 dB is enough. The noise factor has to be the most possible low and their values are normally close to 20 or 15 dB.

2.4.1 Principal Mixers Points of study

Some points that are important to discuss in this chapter such as:

Conversion Gain

The conversion gain represented in Figure 12 [1] as the name refers, it is a ratio between the values of the frequency wished and the frequency that has as source the LNA. These values can be given in magnitude or db. It is possible to assume the equation 2.14 [1]:

$$Conversion\ Gain = 20 * \log_{10}\left(\frac{value\ at\ fIF}{value\ at\ fRF}\right) \quad \textbf{(2.14)}$$

The values at fIF (intermediate frequency) and at fRF (radio frequency) in these conditions have to be in magnitude.

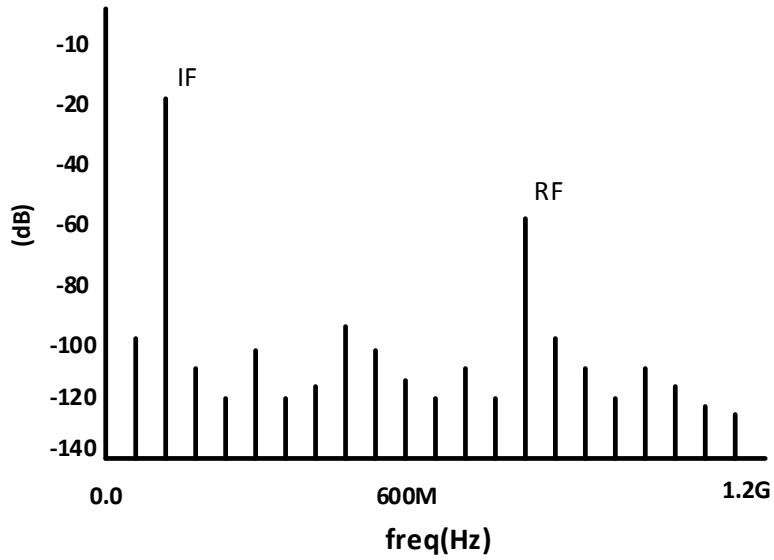


Figure 10-Conversion Gain.

Noise Factor

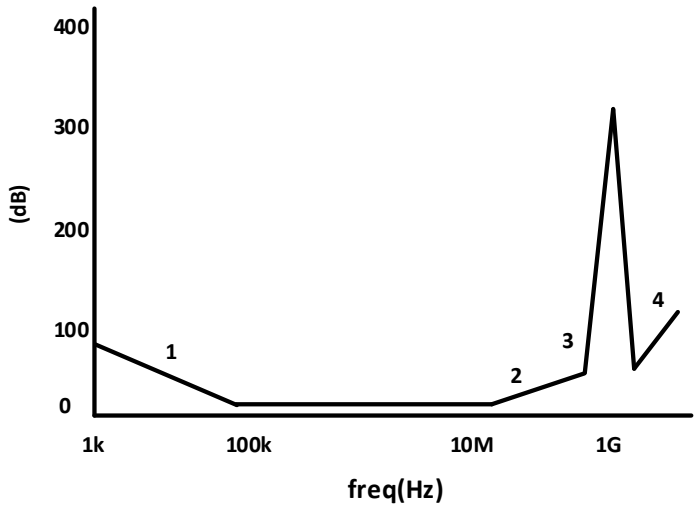


Figure 11-Noise Factor.

In relation to noise factor, it is possible to see four zones, which is seen in Figure 11 [1, 2] is extremely important when it is required to analyze the performance of a Mixer [1].

1. $\frac{1}{f}$ noise
2. Noise Figure increasing due to drop in conversion gain
3. $\frac{1}{f}$ noise mixing up to the LO
4. $\frac{1}{f}$ noise mixing up to second harmonic of the LO

As was seen previously, this $\frac{1}{f}$ noise represents the flicker noise and one of the targets, when it is required to optimize the best global noise factor, is tried to reduce at the maximum the flicker noise for the frequency work which can be 10, 20 or 40MHz.

2.4.2 Passive Mixer

There are two types of mixer, the passive and the active. The first does not have gain but has some advantages such as, no DC current in quad implies that there is no flicker noise, the linearity is really good since the output signal is a current and the voltage swing does not limit the linearity of the Mixer. The op-amp output stage can be converted into an IF filter. Obviously that this op-amp required some extra power, more consumption and introduces additional noise. It is also true that this kind of configuration needs large LO drive compared with other topologies like active Gilbert Cell and needs a common mode feedback circuit at the input of the op-amp. Speaking more specifically, the best way to produce the mixing operation is to use a switch and this process consists in transferring the input RF signal to the output at the LO frequency [16].

When the LO signal is at high level, the switch is open and the input is transferred, but when the LO signal is at low level the input does not have the same way. This switch can be done, using MOS transistors that is shown in Figure 12 [1] and basically it will force the transistor swing between cut-of region when the switch is open (transistor not conducting) and saturation or triode region when the switch is close(transistor conducting).

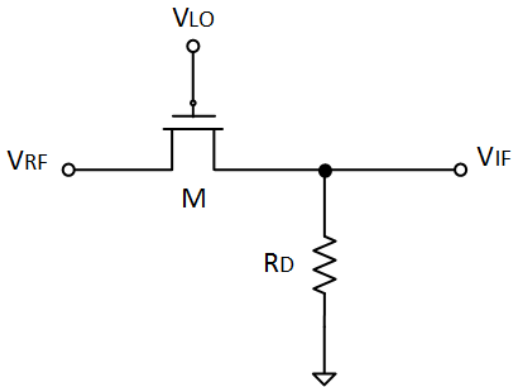


Figure 12-Passive Mixer.

This mixer is implemented with an active device, a MOS transistor operating in triode region, since in triode, the transistor has to be modified as a low impedance resistor.

2.4.3 Active Mixer

There are two simple and good alternatives that can provide gain and therefore they are commonly used in RF systems that can be shown in Figure 15 [1] and Figure 16 [1]. The big difference is related with the configuration, instead of use a single active device, is used a differential pair because the mixing operation is achieved through the same commutation behavior. These transistors, when active, will operate in the saturation region where they supply current gain and a high output impedance much larger than the output load. The first architecture is the single balanced mixer and in this case, the RF input is converted into a current by the transconductance stage.

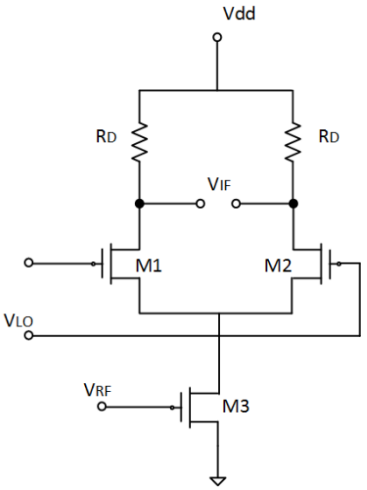


Figure 13-Active Mixer 1ºArquitecture.

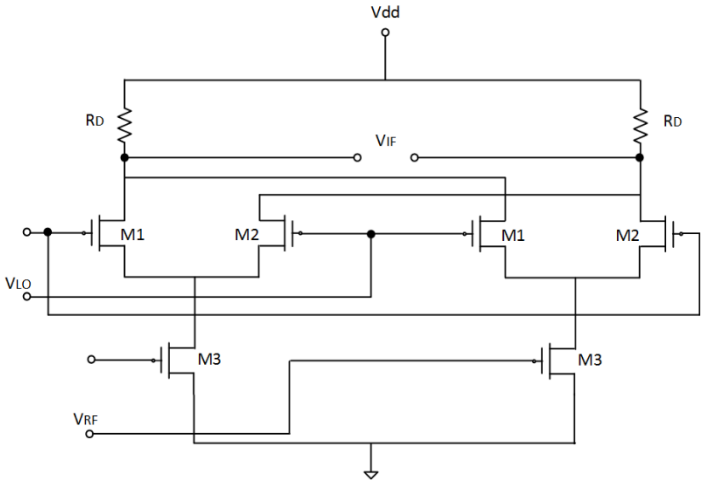


Figure 14-Active Mixer 2ªArquitecture.

This second architecture has the conversion gain as single balanced mixer but has also some advantages such as, better linearity, better port-port isolation, less sensitive to even order distortion and due to his symmetry, it removes the LO harmonic from the output. However there are too some disadvantage such as, more area and large power consumption.

Chapter 3

Low Voltage and Wideband Techniques for LNA and Mixer

There are some techniques that are crucial to obtain low voltages values and wideband frequency, and one of them are the DTMOS and the Wideband configuration, replacing a resistor by a transistor. With these techniques, it is possible to achieve for the supply voltage, 0.4 V and for the GBW 2.4, 5GHz with good gain and noise factor. Obviously that to obtain these performances, it is mandatory to do an heavy mathematic work to explore and discover all the equations, which depend of many factors.

3.1 Mosfet Operation Under Low Voltage Conditions

It is used some techniques to obtain a good performance when the goal, it is try to reduce at the maximum, the supply voltage. The DTMOS technique was first introduced in 1994 [8]. Since then many novel circuit applications of this technique have been proposed. The DTMOS technique is mostly used in digital applications in which the gate and the body of the MOSFET are tied together, which it is seen in Figure 15. In this case V_{th} is high at V_{GS}=0, but reduces when the device turns on, thus facilitate the inversion layer formation, near the interface between the oxide and the bulk substrate [15].

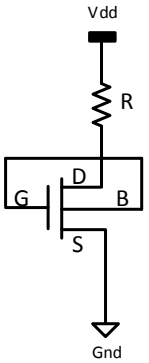


Figure 15-DTMOS Configuration.

$$V_{Th} = V_{TO} - \gamma * \left(\sqrt{\phi_0} - \sqrt{\phi_0 - V_{BS}}\right) =$$

$$= V_{TO} - \gamma * \left(\sqrt{\phi_0} - \sqrt{\phi_0 - V_{GS}}\right) \quad \textbf{(3.1)}$$

On the other hand the threshold voltage of the device is a function of his gate voltage, as the gate increases the threshold voltage, Vth drops resulting in a much higher current drive than standard MOSFET for low-power supply voltages, allowing the circuit works at 0.6 V with a bigger gm and consequently more gain. It is also possible to use the DTMOS technique in bulk CMOS technology for analog circuit applications. The equation 3.1 [1] and equation 3.11 [1] are associated with this explanation.

$$g_m = \mu C'_{ox} \frac{W}{L} (V_{GS} - V_{Th}) \quad \textbf{(3.11)}$$

3.2 Wideband configuration for Amplifiers

In a traditional LNA, the typical I/V conversion implemented at the output mode is usually a LC Tank circuit, which guaranties a narrowband response. However the same I/V operation can be obtained by a simple resistor, activating a wideband characteristic. One of the problem associated with this approach under low voltage supply constraints, is the DC voltage drop at the resistor, that can't be compatible with the available total voltage headroom. To solve this problem is replaced a resistor by a transistor in triode region, but the V_{DS} value in AC has to be smaller than the V_{RD} in DC [15, 21].Equation 3.12 [1] is associated with this explanation.

$$I_D = \mu C'_{ox} \frac{W}{L} \left[(V_{GS} - V_{Th}) V_{DS} - \frac{1}{2} {V_{DS}}^2 \right] \quad \textbf{(3.12)}$$

If it is assumed either a value for the transistor size and how is possible to calculate the V_{RD}, through DTMOS the value of V_{DS}, is can be easily changed regulating the transistor size. It is known that V_{DS} depend on V_{th} but V_{th} depend on V_{BS} so it is important to see the impact of V_{th} on V_{BS}. It is seen at the Figure 16 that V_{th} practically does not change in order to V_{BS} which prove a better performance if it is used transistors instead of resistors. Other advantage of use transistors, it is the fact to be possible to work with the bulk or the gate and connect there a voltage control to tune the gain as is seen in the Figure 17.

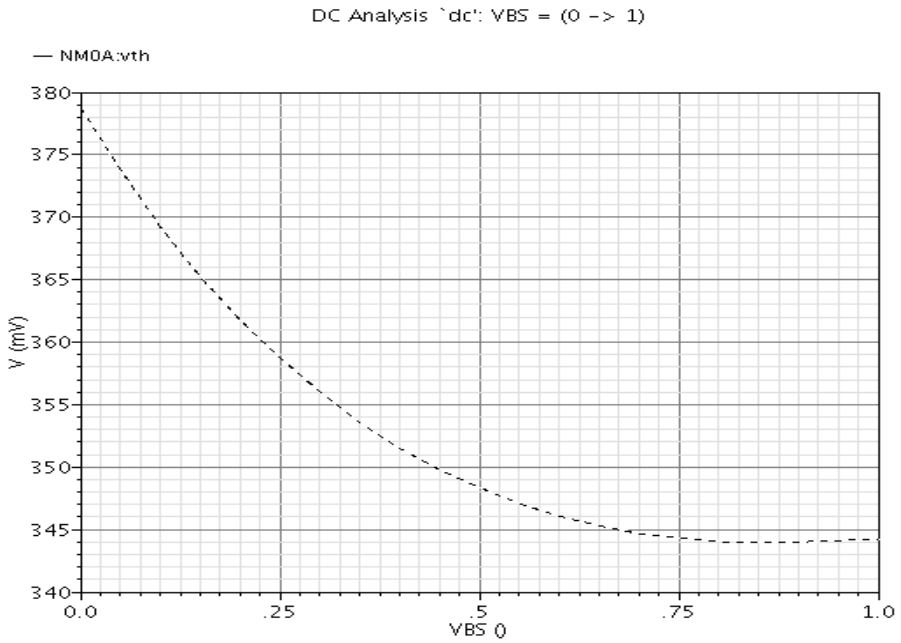


Figure 16-Vth in function of Vbs.

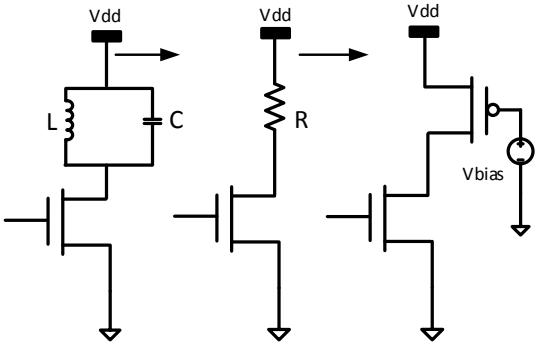


Figure 17-Resistor Replaced by Transistor.

It is quite important to note that these techniques are crucial to the low voltage and low consumption, but it is also significant to understand that many times are needed others processes to make a circuit operable and stable, thus the DTMOS and the wideband transformations are fundamental but do not solve all the problems surrounding.

3.3 Typical Balun LNA

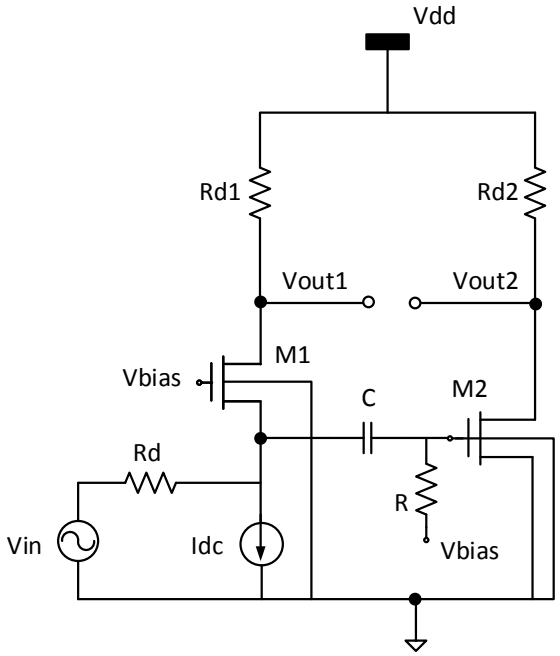


Figure 18-Balun LNA.

The circuit showed in Figure 18 [17] is a balun LNA, in which the thermal noise of M_1 (main source of noise) is cancelled out [18]. The noise produced by M_1 appears in phase at the two terminals, while the signals at these terminals are in opposition. Therefore, the gain is doubled and the noise is cancelled in the harmonic's pair. It can be shown, that the distortion introduced by M_1 is also cancelled [9].

The differential voltage gain of the LNA is obtained from the gain of a common-gate (CG) stage plus the gain of the common-source (CS) stage how is shows in equation 3.13 [17].

$$A_v = g_{m1}Rd1 + g_{m2}Rd2 \quad \textbf{(3.13)}$$

As shown in the Fig. 4, the gain of the two stages should be equal for balanced balun operation and for noise and distortion cancellation [18]. The maximum gain is limited by the value of the resistors since g_{m1} is set by the input matching. This equation is crucial to understand how to achieve a better gain, but obviously it is normal if it is lost something in others aspects.

3.4 Proposed Balun LNA

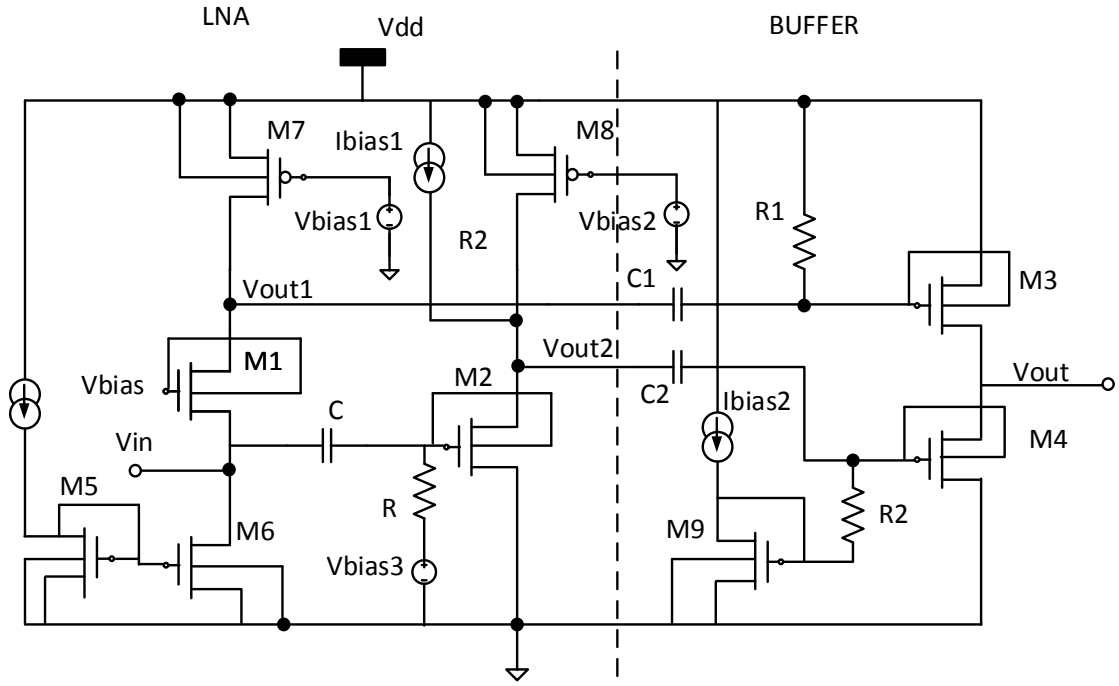


Figure 19-Proposed LNA.

The circuit in the Figure 18 [17] cannot operate at 0.6 V with good gain and it is limited, therefore it is proposed a solution to solve this limitation. It is replaced the resistor load by transistors in triode region and it is used DTMOS in M1, 2, 3, 4 as it is possible so see in the figure above. In the proposed LNA showed in Figure 19, a $vbias_{1,\,2,\,3}$ and DTMOS are used to reduce the noise factor, boost the gain and to be possible to make this circuit work between 0.6 V - 1.2 V. The buffer was used to make the conversion from differential to single ended. It is possible to obtain the gain expression doing the small signal analyses of the first stage looking for the Figure 20 :

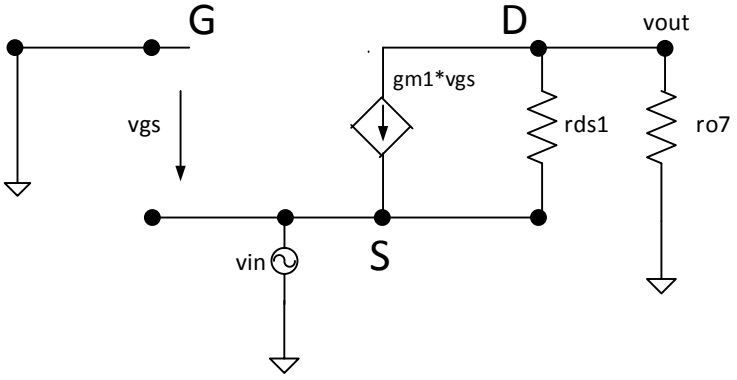


Figure 20-First Stage Small-Signals.

$$rds = \frac{1}{gds} \qquad V_{GS} = -V_{in}$$

$$g_{07} * V_{out} + g_{ds1} * (V_{out} - V_{in}) - g_{m1} * V_{in} = 0$$

The final gain of each stage is given by equation 3.14:

$$A_v = \frac{V_{out}}{V_{in}} = g_{m1} * r_{07} \tag{3.14}$$

It was seen before that this circuit has two stages, a CG and CS, thus:

The gain of the proposed LNA as active load is given by equation 3.15:

$$A_v = g_{m1} * r_{07} + g_{m2} * r_{08} \tag{3.15}$$

It is known that $R_{in} = \frac{V_{in}}{I_{in}}$

Through the deductions done before it is also known that:

$$R_{in} = \frac{V_{in}}{I_{in}} = \frac{1}{g_{ds1} + g_{m1}} + \frac{r_{07}}{(g_{ds1} + g_{m1}) * r_{ds1}}$$

The input resistance is given by equation 3.16:

$$\frac{r_{07}}{(g_{ds1} + g_{m1}) * r_{ds1}} \approx 0 \tag{3.16}$$

The final input impedance is given by equation 3.17:

$$R_{in} = \frac{1}{g_{m1}} \tag{3.17}$$

It is also important to study the output impedance and the output frequency pole.

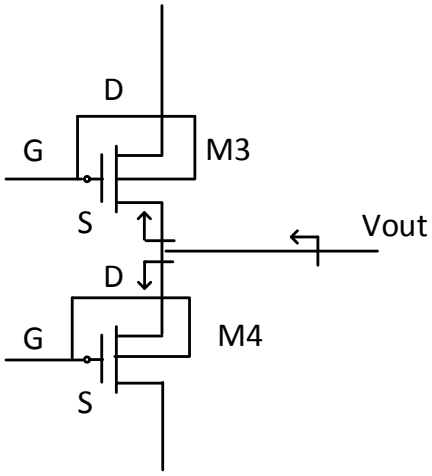


Figure 21-Buffer Output.

Doing a simple analyse of this circuit shown in Figure 21, it is easy to understand that the output impedance is given by equation 3.18.

$$r_{out} = r_{ds3} // r_{ds4}$$

$$r_{out} = \frac{1}{g_{ds4} + g_{ds3} + g_{m3}} \approx \frac{1}{g_{m3}} \tag{3.18}$$

Knowing the output impedance is simple to obtain the output frequency pole.

The output frequency pole is given by equation 3.19.

$$\omega_{pout} = \frac{1}{g_{m3} * \left[c_{gs3} + c_{sb3} + c_{gd4} + c_{db4}\right]} \tag{3.19}$$

The body effect was unvalued due to the fact of $g_{mb1}, g_{mb2}, g_{mb3}, g_{mb4}$ be too small in relation to correspondentg_m as it is shown in Table 1.

Table 1-Transistors gm values.

At 1.2 V					
gm	Value (mS)	gm	Value (mS)	gds	Value (mS)
gm1	25	**gmb1**	1.3	**gds7**	10
gm2	30	**gmb2**	2.7	**gds8**	5
gm3	6.5	**gmb3**	0.6		
gm4	6	**gmb4**	0.55		

If it is assumed that $g_{m1} = g_{m2} = g_m$ [17], the noise factor is expressed by equation 3.20 [17].

$$F_{LNA} = 1 + \frac{k_f}{8kTR_S cox f^{\alpha f}}\left(\frac{1}{W_1 L_1} + \frac{1}{W_2 L_2}\right) + \frac{\gamma}{2R_{Sgm}} + \frac{1}{R_S ropgm^2} \quad \textbf{(3.20)}$$

where k is Boltzmann's constant, cox is the oxide gate capacitance per unite area, Wi and Li are the transistor dimensions , T is the absolute temperature, γ is the excess noise factor, kf and αf are intrinsic process parameters, which depend on the size of the transistors [10, 11].

3.5 Single end Mixer design

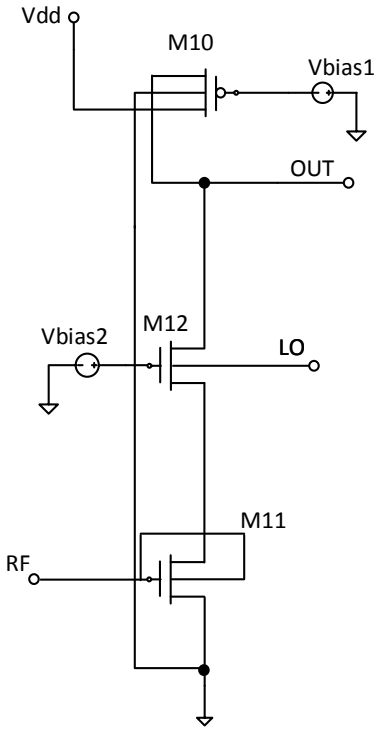


Figure 22-Proposed Mixer.

It is possible to verify that are used two voltage controller, both with the same duty, make real the polarization of each transistor with some kind of values in volt. Without this technique would be impossible or extremely difficult add gain to this system even at 1.2 V.

This circuit presented in Figure 22 represents a telescopic cascode topology and it is easy to know that the input impedance is given by:

$$R_{in} = \infty$$

because the impedance it is seen by the gate.

In this case, the transistor M12 only works as switch for a LO signal sufficiently strong, otherwise the transistor M11 is the only responsible for the transconductance and consequently, the main factor for the gain.

The gain of the proposed Mixer is given approximately by equation 3.22:

$$A_v = \frac{V_{out}}{V_{in}} = \frac{1}{\pi} * (g_{m11} + g_{m11b}) * R10 \quad \textbf{(3.22)}$$

$$A_v = \frac{V_{out}}{V_{in}} = \frac{g_{m11} + g_{m11b}}{\pi * gds_{10}} \quad \textbf{(3.23)}$$

Chapter 4

Proposed Balun LNA and Mixer Simulations

4.1 LNA Simulations

The objective of this chapter is show all the possible simulations and prove that the low voltage techniques enounced in the chapter three had a big role for this project. First will be showed records for the LNA and the Mixer separately and then for the combined LNA plus Mixer. All circuits presented in this document, and specifically in this chapter, were simulated using supply voltages at 0.6 and 1.2V to 450,600 and 900MHz. First of all, the simulations will be done with this configuration:

1. TT Model transistors at 0º,27º and 85º
2. SS Model transistors at 0º,27º and 85º
3. FF Model transistors at 0º,27º and 85º

This configuration will be follow, because the circuit has to have the reliability to operate in any part of globe, therefore it is interesting to see their diverse performances in three different type of temperature. In general were not made all the possible simulations, but only the priority in our understanding.

All simulations were done in Cadence software and for all measurements done in this thesis, some analyses such as PSS, PSS and PNOISE, PSS and PXF, Swept PSS, Swept PSS and PAC and PSS and Swept PAC were chosen.

Transistors size at 1.2 V

Table 2-Transistors size at 1.2 V.

Device	Width(μm)	Length(nm)	Finger Number	Multiplier	Size(μm)
M1	7.2	120	4	10	288
M2	7.2	120	4	20	576
M3	4	120	4	9	144
M4	4	120	4	9	144
M5	1.8	120	13	1	23
M6	1.8	120	7	1	13
M7	1.6	240	3	16	77
M8	6	120	4	5	108
M9	1.8	120	8	1	14

DC Operating Points at 1.2 V

Device	Vds (mV)	Vdsat (mV)	Work Region
M1	130	70	Saturation
M2	700	80	Saturation
M3	378	86	Saturation
M4	800	85	Saturation
M5	600	200	Saturation
M6	100	200	Triode
M7	350	420	Triode
M8	255	290	Triode
M9	450	75	Saturation

Transient Simulations at 1.2 V

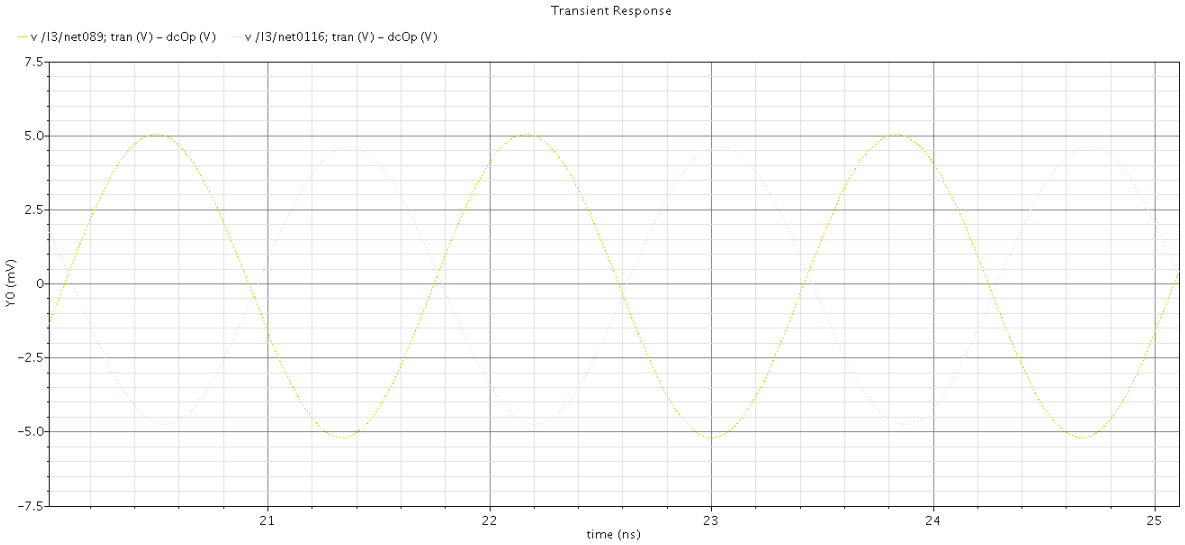


Figure 23-Transient Simulations at 1.2 V.

Phase Simulations at 1.2 V

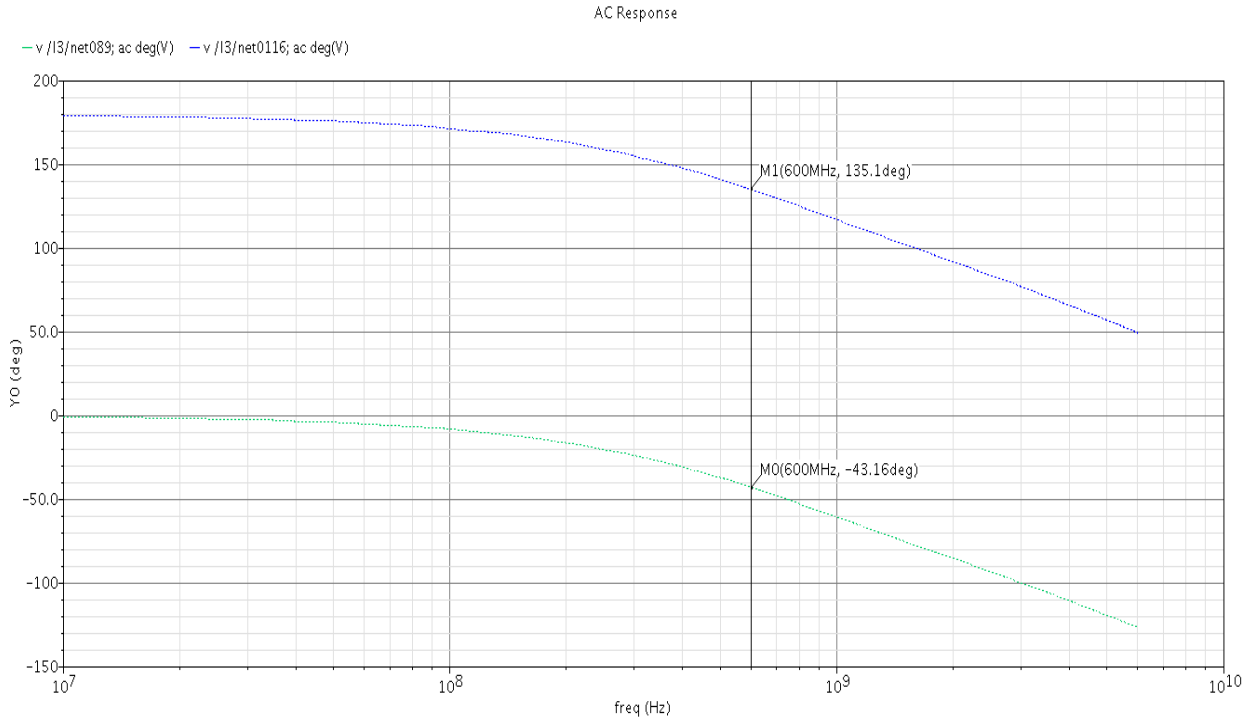


Figure 24-Phase Simulation at 1.2 V.

Gain Simulations at 1.2 V

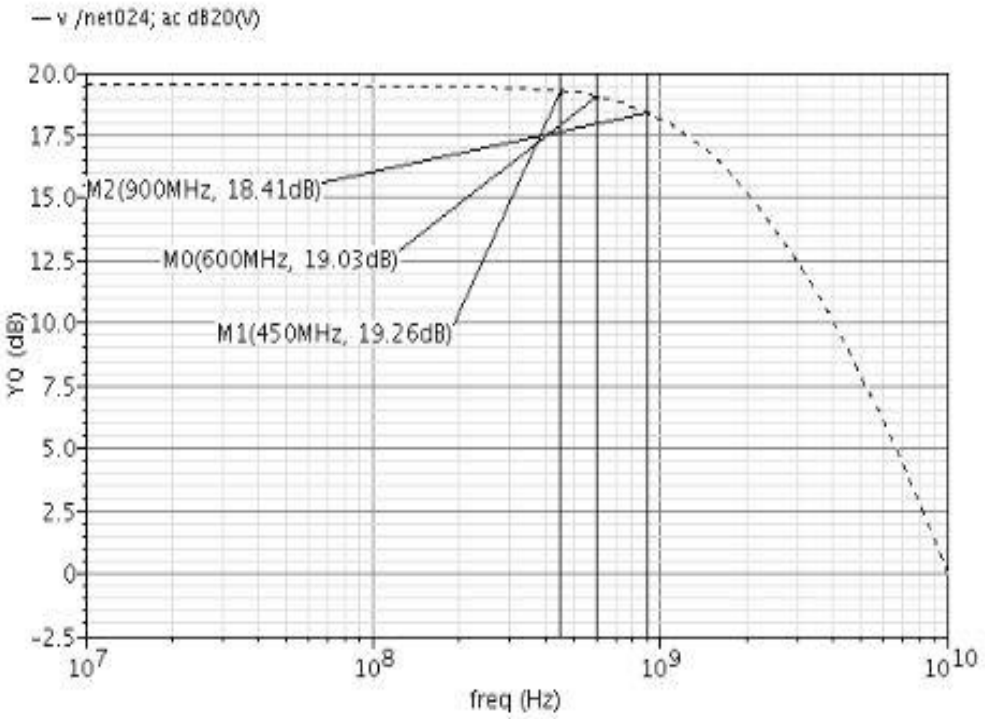


Figure 25-Gain Simulations at 1.2 V.

Noise Factor Simulations at 1.2 V

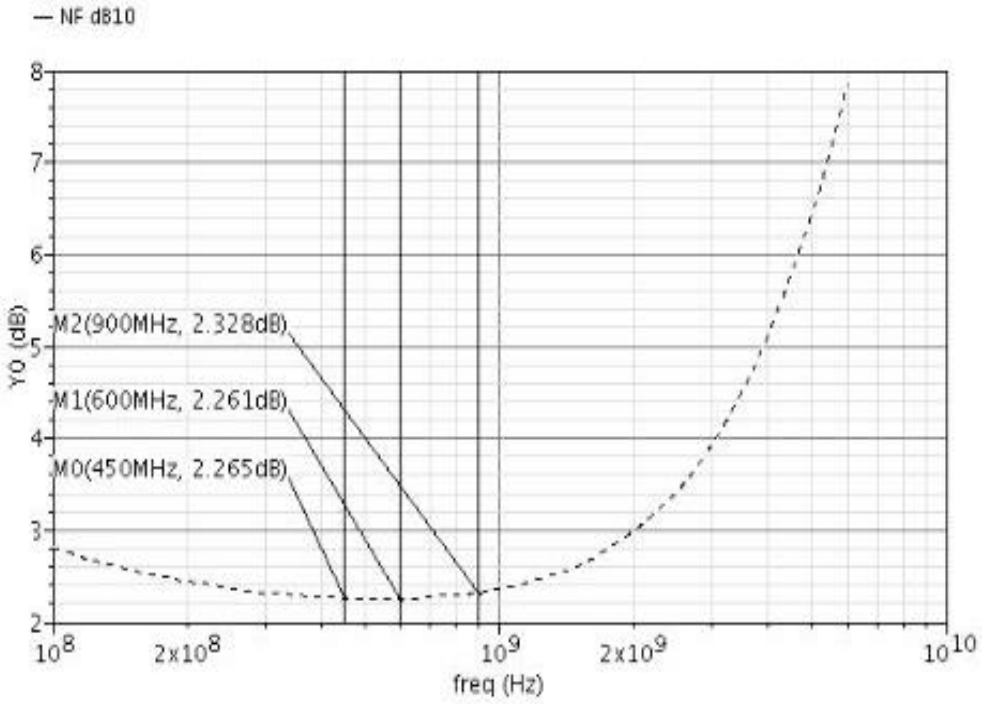


Figure 26-Noise Factor Simulations at 1.2 V.

S11 Parameter Simulations at 1.2 V

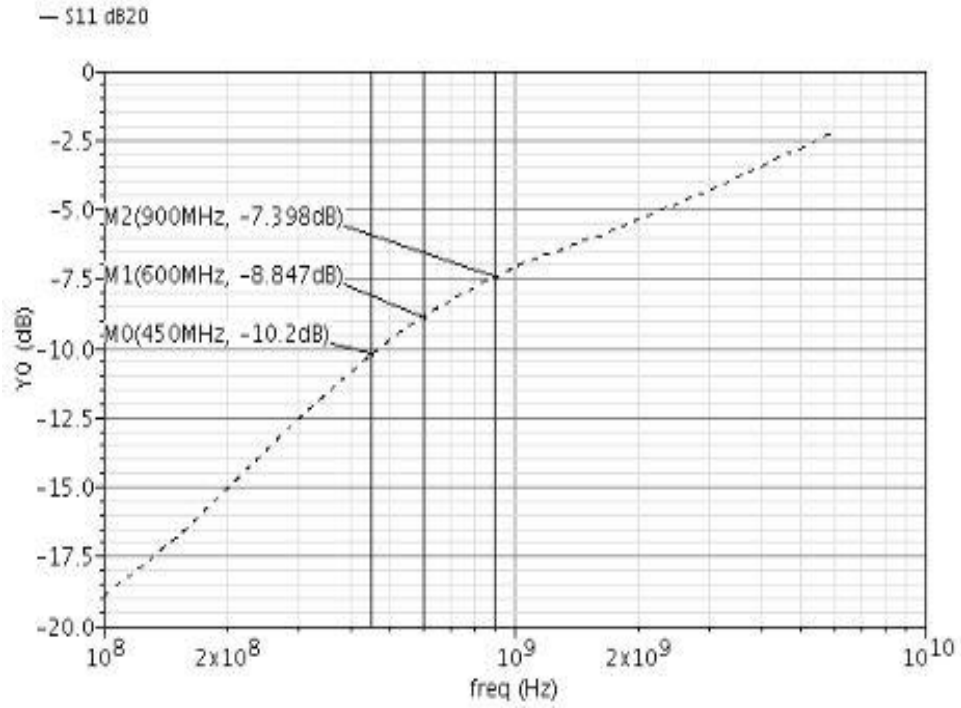


Figure 27-S11 Parameter Simulations at 1.2 V.

The transient and phase simulations were done with the objective to verify the balance between stages, it is possible to note through Figure 23 and Figure 24 that each stage has practically the same gain and both responses are delayed of 180º, which demonstrate that the circuit is working correctly. For the gain and the noise factor were achieved respectively to 450MHz 19.26 dB and 2.26 dB which are good results, but to obtain it, was mandatory to follow the rules related to the working region of each transistor. The S11 parameter values showed in Figure 27 are not the best but for our working range, 450MHz to 900MHz are quite reasonable.

Table 3-Results at 1.2 V.

1.2 V						
Frequency(MHz)	AV	NF	1dB Compression	IIP2	IIP3	PDC(mW)
450	19.26	2.265				
600	19.03	2.261	-12.2	-5.8	-11.2	11.8
900	18.41	2.368				

Transistors size at 0.6 V

Table 4-Transistors size at 0.6 V.

Device	Width(µm)	Length(nm)	Finger Number	Multiplier	Size(µm)
M1	7.2	120	4	10	288
M2	7.2	120	4	20	576
M3	4	120	4	9	144
M4	4	120	4	9	144
M5	1.8	120	13	1	23
M6	1.8	120	7	1	13
M7	1.6	240	3	16	77
M8	5.4	120	4	3	65
M9	1.8	120	8	1	14

DC Operating Points at 0.6 V

Table 5-DC Operating Points at 0.6 V.

Device	Vds (mV)	Vdsat (mV)	Work Region
M1	40	153	Triode
M2	520	64	Saturation
M3	350	47	Saturation
M4	252	75	Saturation
M5	610	194	Saturation
M6	77	180	Triode
M7	479	304	Saturation
M8	82	270	Triode
M9	353	66	Saturation

Gain Simulations at 0.6 V

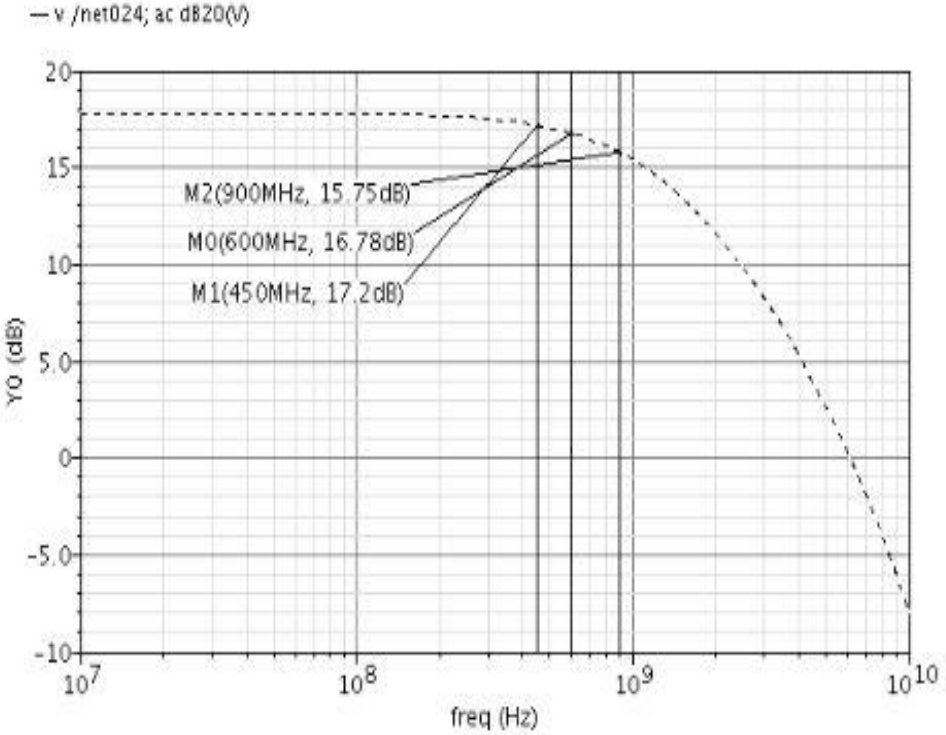


Figure 28-Gain Simulations at 0.6 V.

Noise Factor Simulations at 0.6 V

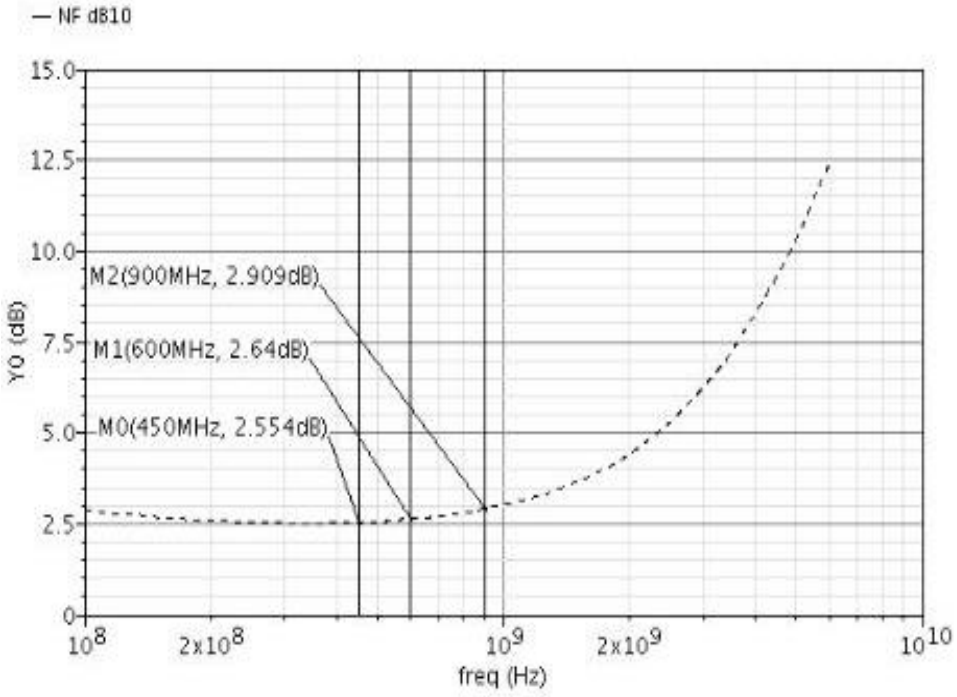


Figure 29-Noise Factor Simulations at 0.6 V.

S11 Parameter Simulations at 0.6 V

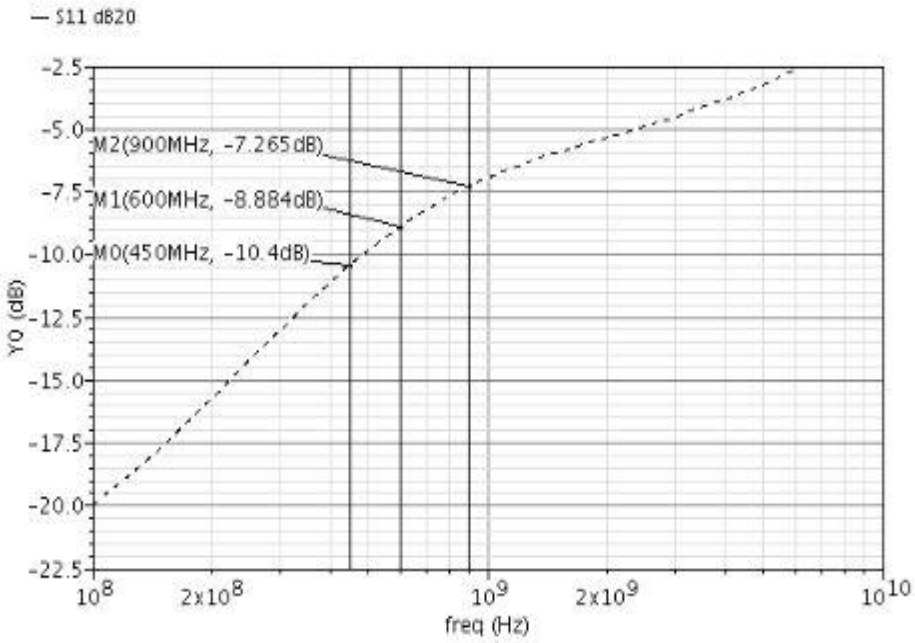


Figure 30-S11 Parameter Simulations at 0.6 V.

IIP3 Simulations

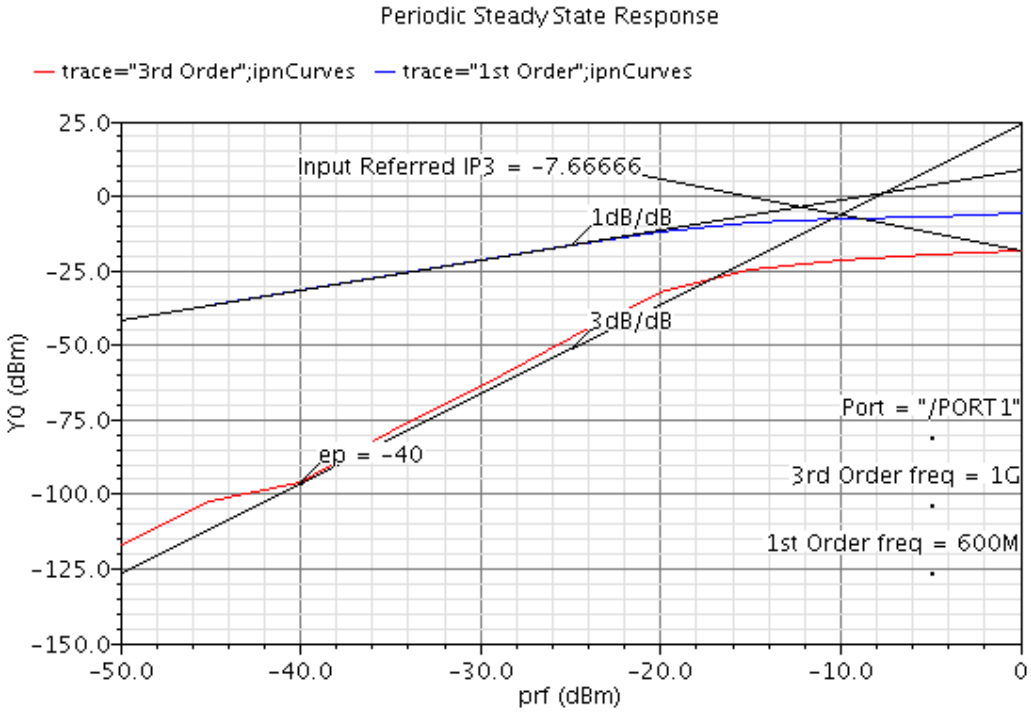


Figure 31-IIP3 Simulations.

PVT Variations at 0.6 V

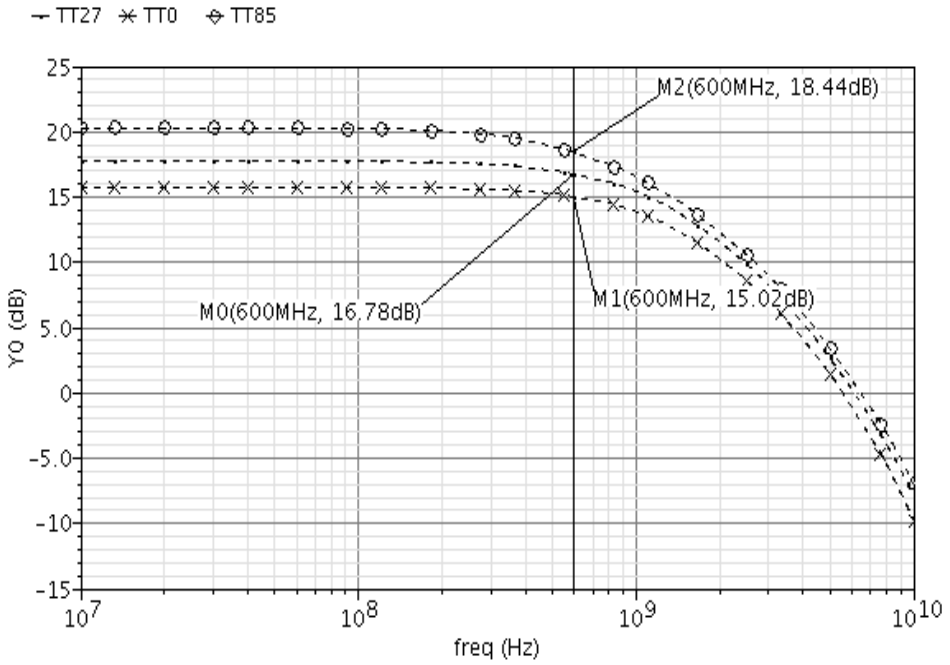
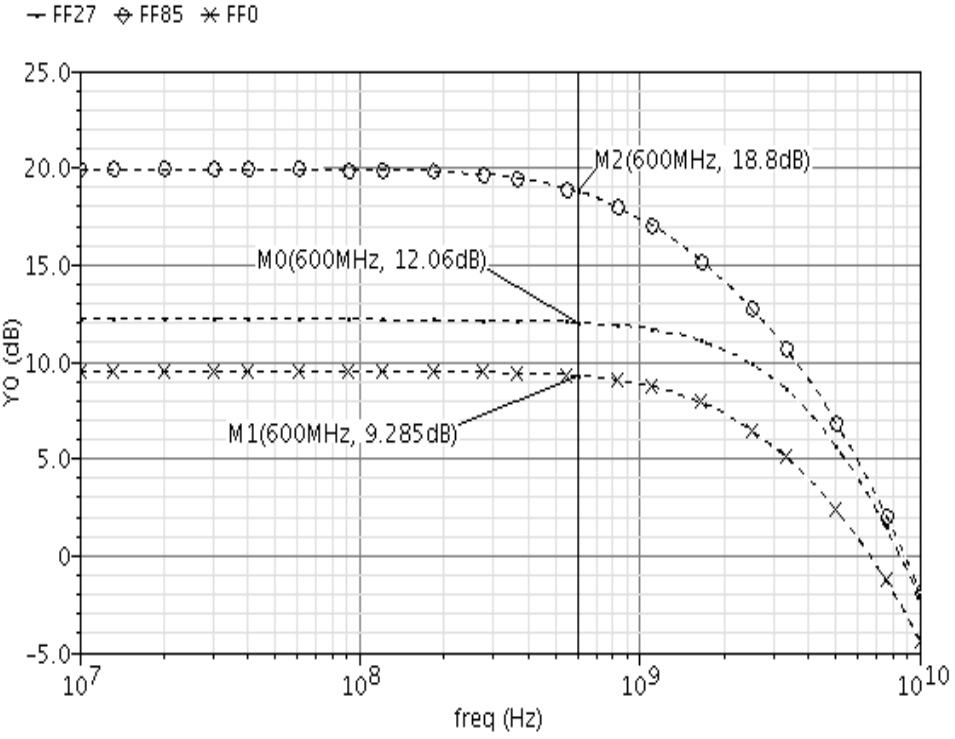


Figure 32-TT Simulations at 0.6 V.



. Figure 33-FF Simulations at 0.6 V

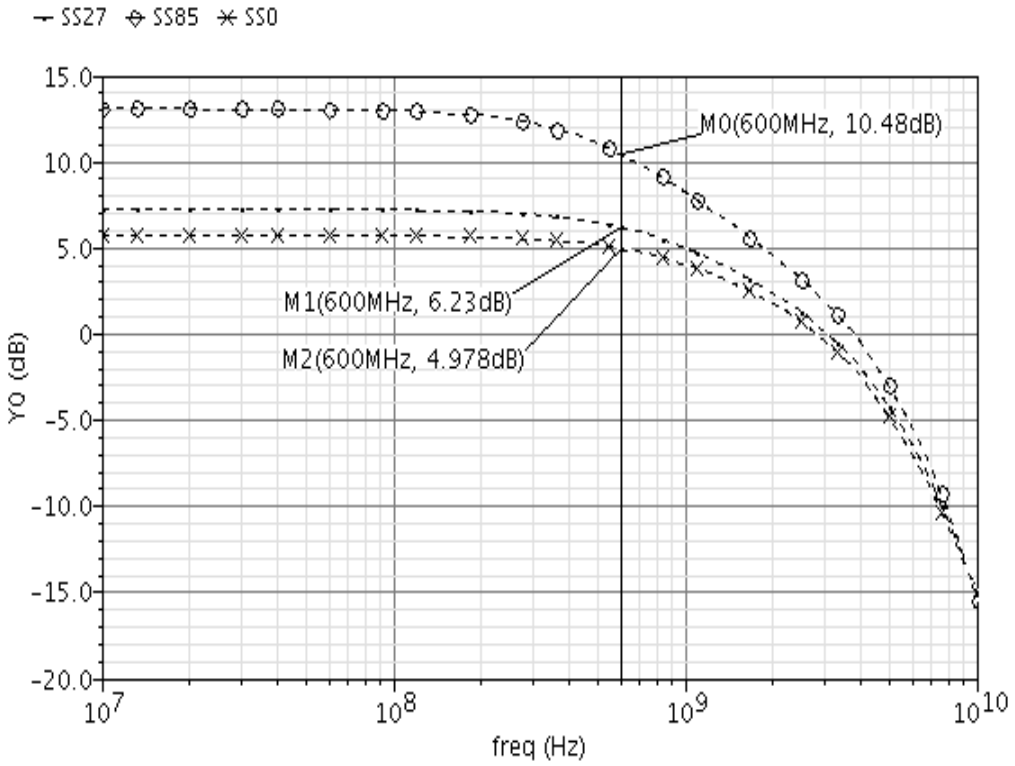


Figure 34-SS Simulations at 0.6 V.

Simulations with and without DTMOS at 0.6 V

Noise Factor:

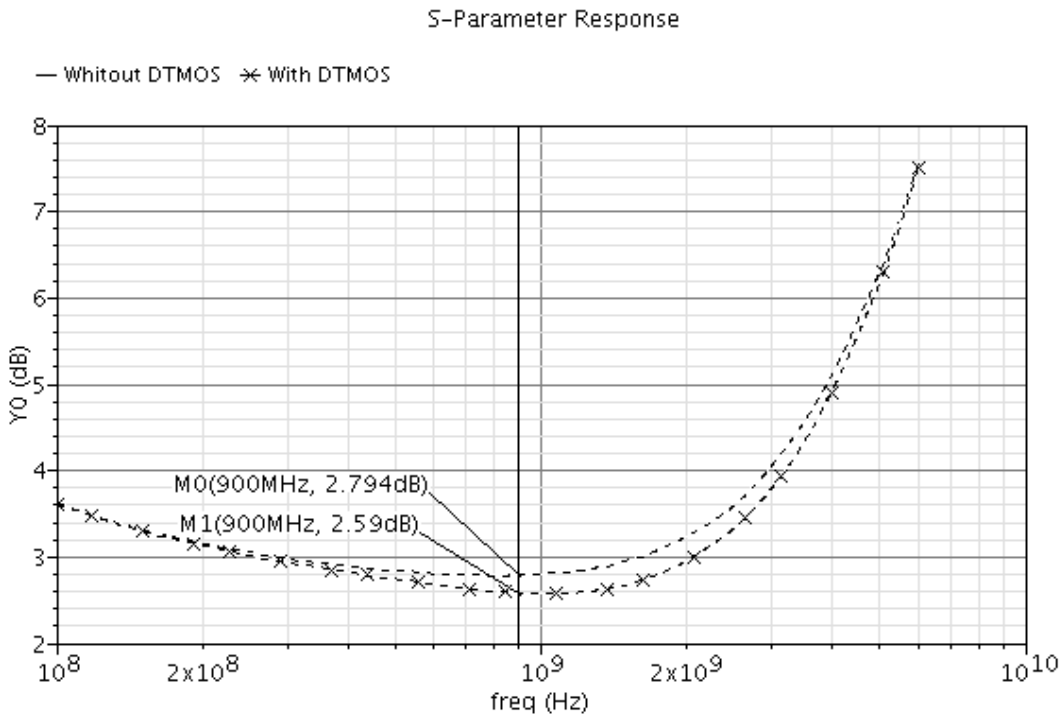


Figure 35-Simulations with and without DTMOS at 0.6 V.

Gain:

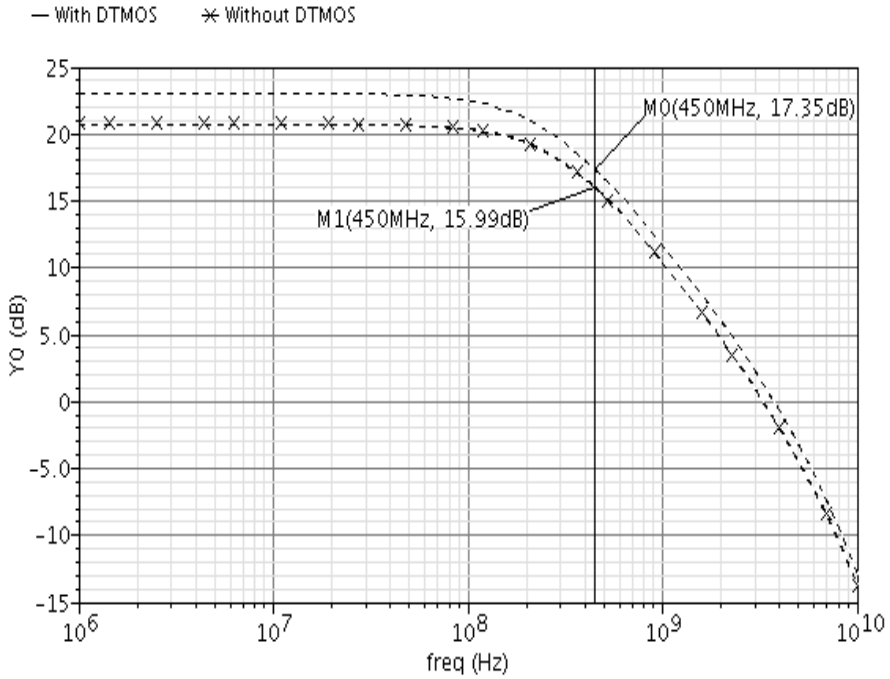


Figure 36-Simulations with and without DTMOS at 0.6 V.

0.6 V	Table 6-Results at 0.6 V.					
Frequency(MHz)	AV(dB)	NF(dB)	1dB Compression	IIP2	IIP3	PDC(mW)
450	17.2	2.554				
600	16.75	2.64	-9.4	-3.3	-7.6	4
900	15.75	2.909				

Table 7-Models Transistors Results.

0.6 V	**600 MHz**				
Models	AV(dB)	**Models**	AV(dB)	**Models**	AV(dB)
TT at 0º	15.02	**FF at 0º**	9.25	**SS at 0º**	4.978
TT at 27º	16.75	**FF at 27º**	12.06	**SS at 27º**	6.23
TT at 85º	18.44	**FF at 85º**	18.8	**SS at 85º**	10.48

It is showed in all different simulations through Figure 28 to Figure 36 and through Table 3**,**Table 6 that were achieved good results, which were only possible with the use of DTMOS. It was obtained to 450MHz for the gain and noise factor respectively 17.2 dB and 2.55 dB. It is note that with DTMOS was achieved almost 1.5 dB in addition in relation to the simulation using MOS, which is crucial to explain in practice why these devices should be used more and more in this kind of work. The results of thermal variation show us the consistent capacity of this circuit work in adverse climates with quality and stability. The S22 parameter simulations were also done but the graphs were not showed in this document due to the fact of the target of this thesis does not be related with the development of a single block named LNA, but yes related with the construction of a structure that it is possible to call LM (LNA+Mixer) and in that way, it is irrelevant to study the output matching.

Finally it is important to note that the simulations, which were done to compare the gain and noise factor with and without DTMOS were realized in different conditions with others transistors size and others voltage controller values.

Table 8-Comparison between DTMOS and MOS.

0.6 V	**450 MHz**	**900 MHz**
Configuration	AV(dB)	NF(dB)
MOS	15.99	2.794
DTMOS	17.35	2.59

These simulations were also done for 450 and 900 MHz to verify the good performance not only with 600 MHz. It was boosted the gain in 1.5 dB and decreased the noise factor in 0.2 dB when are used DTMOS instead of the simple MOS as it is possible to see in Table 8.

4.2 Mixer Simulations

Gain Simulations at 1.2 V

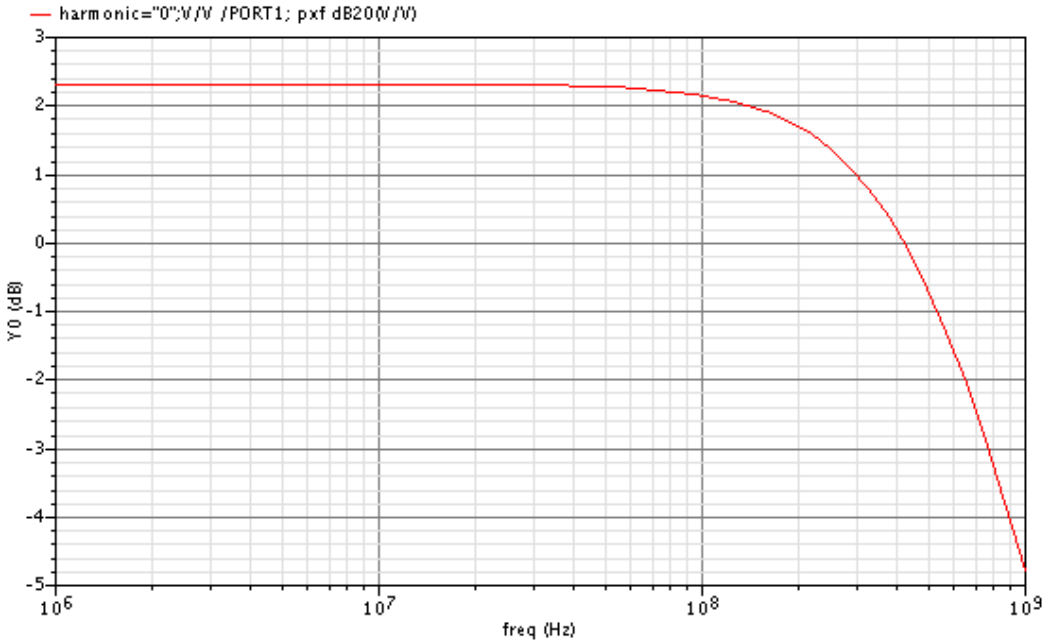


Figure 37-Gain Simulations at 1.2 V.

Noise Factor Simulations at 1.2 V

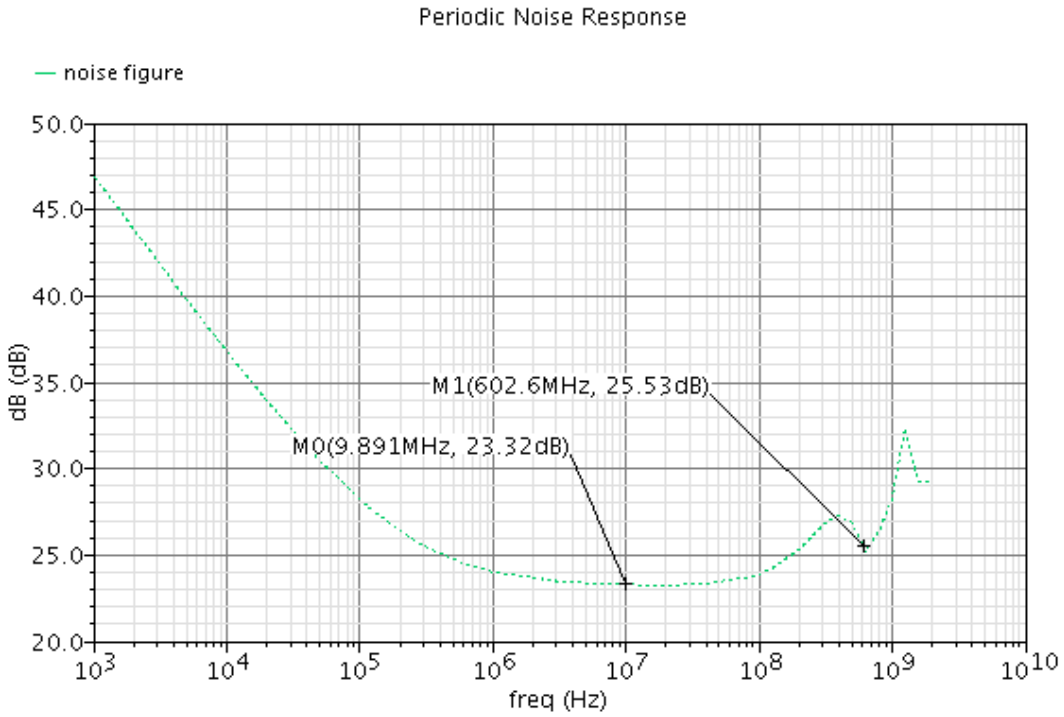


Figure 38-Noise Factor Simulations at 1.2 V.

Transistors size at 1.2 V

Table 9-Transistors size at 1.2 V.

Device	Width(µm)	Length(nm)	Finger Number	Multiplier	Size(µm)
M10	2.4	240	4	1	9.6
M11	5	240	4	30	600
M12	7.2	170	4	5	144

DC Operating Points at 1.2 V

Table 10-DC Operating Points at 1.2 V.

Device	Vds (mV)	Vdsat (mV)	Work Region
M10	229	2	Saturation
M11	3	76	Triode
M12	2	218	Triode

Through the Figure 37 and Figure 38, it is possible to see that were obtained good results for both parameters at 1.2 V but, obviously that this Mixer is too simple and consequently limited. When the simulations are done at 0.8 and 0.6 V, the circuit does not have gain but remains stable, the noise factor acceptable and the consumption is very low compared with others Differential Mixers which could be proposed. The target always passed by the development of a low voltage receiver that was simple and had good results, therefore this was the right choice. Through Table 9 and Table 10 is possible to see the sizing and the DC operating points.

Chapter 5

Design and Simulations of a Combined LNA and Mixer

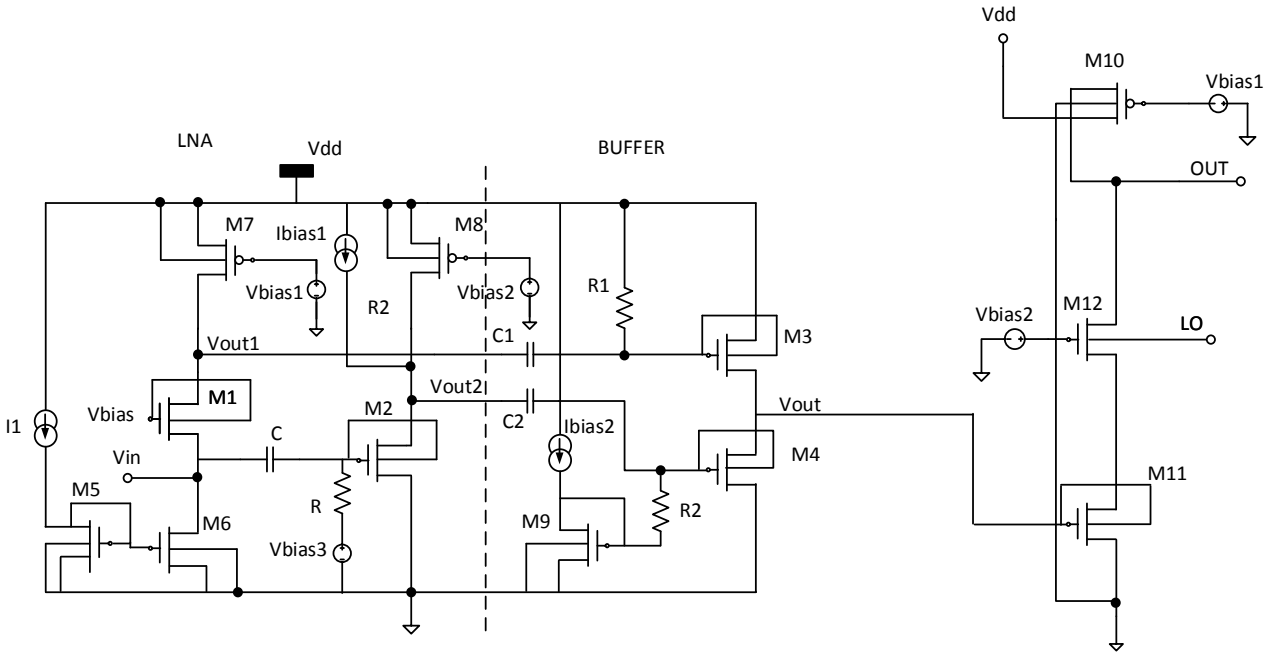


Figure 39-LNA+MIXER.

All circuits presented in this document, and specifically in this chapter as the Figure 39, were simulated using supply voltages at 0.6, 0.8 and 1.2V to 450,600 and 900MHz. First of all, the simulations will be done with this configuration:

1. TT Model transistors at 0º,27º and 85º
2. SS Model transistors at 0º,27º and 85º
3. FF Model transistors at 0º,27º and 85º

This configuration will be follow, because the circuit has to have the reliability to operate in any part of globe, therefore it is interesting to see them diverse performances in three different type of temperature. In general were not made all the possible simulations, but only the priority in our understanding.

Transistors size at 1.2 V

Table 11-Transistors size at 1.2 V.

Device	Width(µm)	Length(nm)	Finger Number	Multiplier	Size(µm)
M1	7.2	120	4	1	28.8
M2	7.2	120	4	20	576
M3	4	120	4	9	144
M4	4	120	4	9	144
M5	1.8	120	13	1	23
M6	1.8	120	7	1	13
M7	1.6	240	3	5	24
M8	6	120	4	4	96
M9	1.8	120	8	1	14
M10	2.4	240	4	1	9.6
M11	5	240	4	30	600
M12	7.2	170	4	5	144

These are the transistors size at 1.2 V, and it is seen through Table 11 that to M2 and M11 was necessary a big value than the others with the objective to balance the stages and consequently boost the total gain.

DC Operating Points at 1.2 V

Table 12-DC Operating Points at 1.2 V.

Device	Vds (mV)	Vdsat (mV)	Work Region
M1	301	125	Saturation
M2	1000	72	Saturation
M3	378	87	Saturation
M4	821	85	Saturation
M5	610	194	Saturation
M6	121	181	Triode
M7	305	488	Triode
M8	155	276	Triode
M9	353	66	Saturation
M10	229	2	Saturation
M11	3	76	Triode
M12	2	218	Triode

As it is seen through Table 12, the M7 and M8 are in triode region and was concluded one more time that for this region were obtained the best results for gain and noise factor in comparison with the saturation zone.

Gain Simulations at 1.2 V

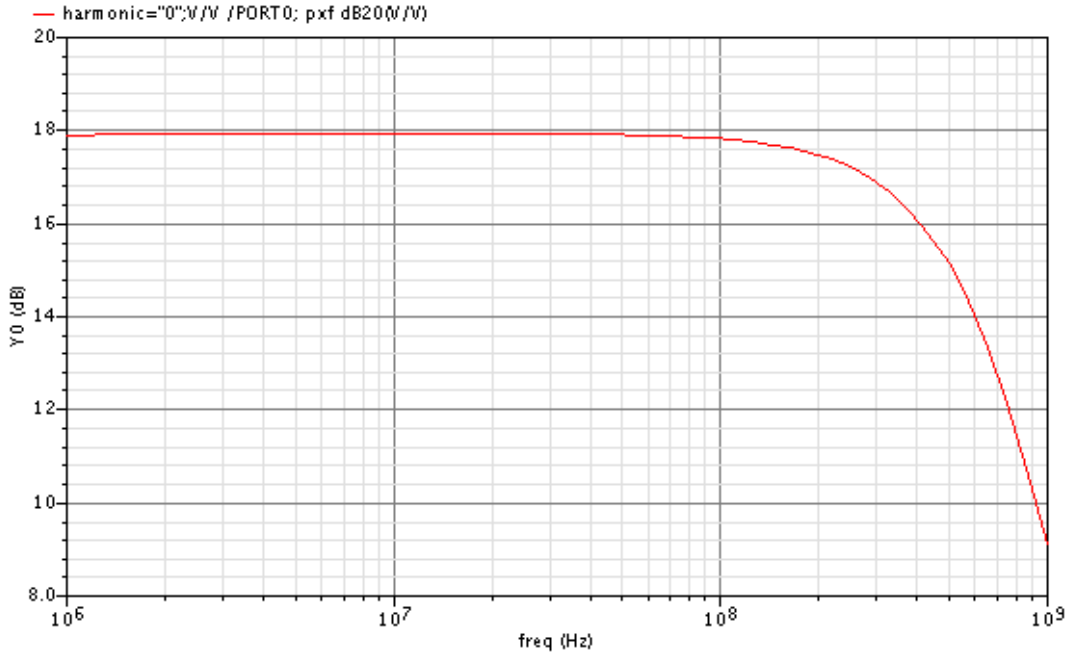


Figure 40-Gain Simulations at 1.2 V.

Noise Factor Simulations at 1.2 V

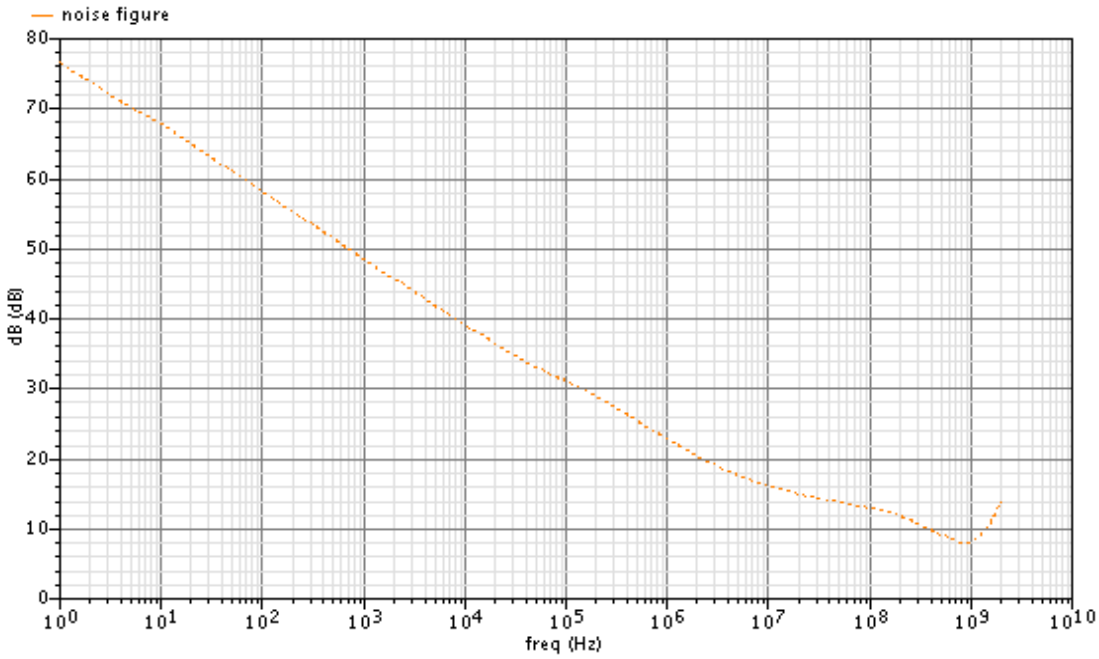


Figure 41-Noise Factor Simulations at 1.2 V.

Transistors size at 0.8 V

Table 13-Transistors size at 0.8 V.

Device	Width(µm)	Length(nm)	Finger Number	Multiplier	Size(µm)
M1	7.2	120	4	1	28.8
M2	7.2	120	4	20	576
M3	4	120	4	9	144
M4	4	120	4	9	144
M5	1.8	120	13	1	23
M6	1.8	120	7	1	13
M7	1.6	240	3	5	24
M8	6	120	4	4	96
M9	1.8	120	8	1	14
M10	2.4	240	4	1	9.6
M11	5	240	4	30	600
M12	7.2	170	4	5	144

These are the transistors size at 0.8 V, and it is seen through Table 13 that to M2 and M11 was necessary a big value than the others with the objective to balance the stages and consequently boost the total gain.

DC Operating Points at 0.8 V

Table 14-DC Operating Points at 0.8 V.

Device	Vds (mV)	Vdsat (mV)	Work Region
M1	779	64	Saturation
M2	629	65	Saturation
M3	378	87	Saturation
M4	821	85	Saturation
M5	610	194	Saturation
M6	9	178	Triode
M7	10	304	Triode
M8	168	277	Triode
M9	353	66	Saturation
M10	2	229	Triode
M11	3	76	Triode
M12	2	218	Triode

As it is seen through Table 14, the M7 and M8 are in triode region and was concluded one more time that for this region were obtained the best results for gain and noise factor in comparison with the saturation zone.

Gain Simulations at 0.8 V

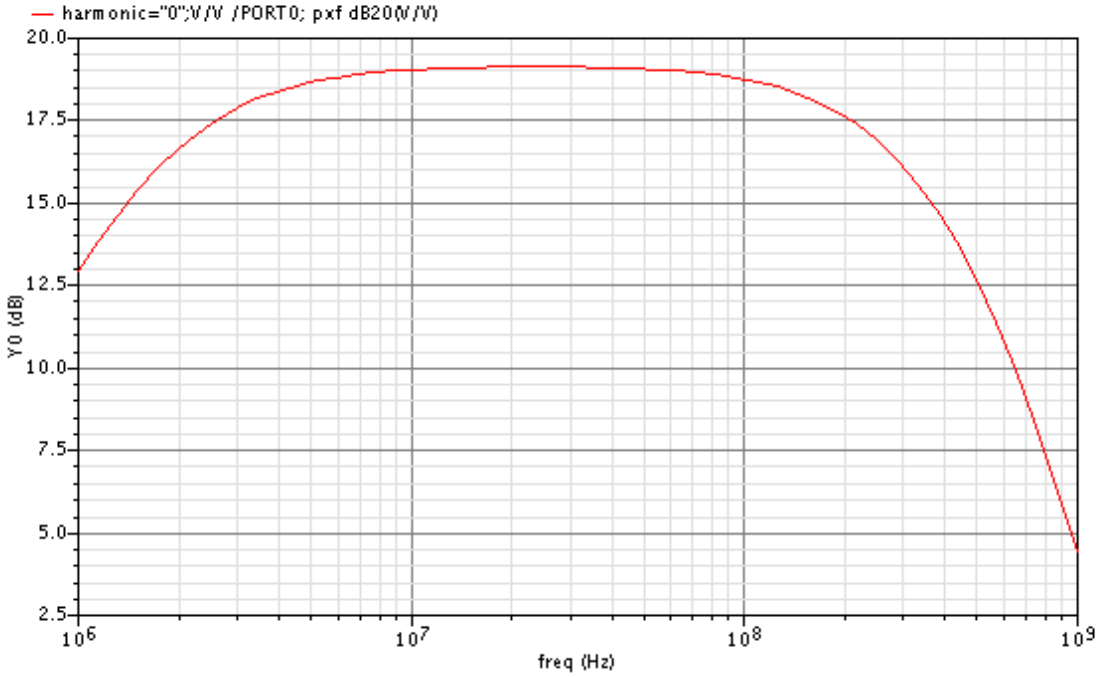


Figure 42-Gain Simulations at 0.8 V.

Noise Factor Simulations at 0.8 V

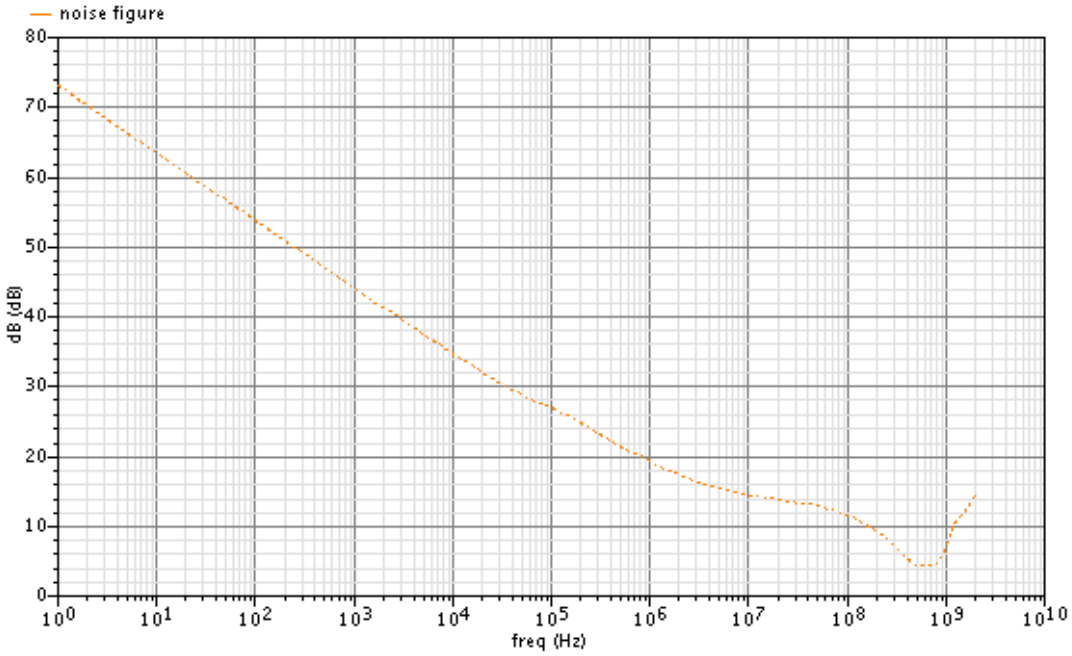


Figure 43-Noise Figure Simulations at 0.8 V.

Transistors size at 0.6 V

Table 15-Transistors size at 0.6 V.

Device	Width(µm)	Length(nm)	Finger Number	Multiplier	Size(µm)
M1	7.2	120	4	1	28.8
M2	7.2	120	4	20	576
M3	4	120	4	9	144
M4	4	120	4	9	144
M5	1.8	120	13	1	23
M6	1.8	120	7	1	13
M7	1.6	240	3	5	24
M8	6	120	4	4	96
M9	1.8	120	8	1	14
M10	2.4	240	4	1	9.6
M11	5	240	4	30	600
M12	7.2	170	4	5	144

These are the transistors size at 0.6 V, and it is seen through Table 15 that to M2 and M11 was necessary a big value than the others with the objective to balance the stages and consequently boost the total gain.

DC Operating Points at 0.6 V

Table 16-DC Operating Points at 0.6 V.

Device	Vds (mV)	Vdsat (mV)	Work Region
M1	11	839	Triode
M2	1000	73	Saturation
M3	378	87	Saturation
M4	821	85	Saturation
M5	610	194	Saturation
M6	120	181	Triode
M7	100	305	Triode
M8	155	276	Triode
M9	353	66	Saturation
M10	1.5	229	Triode
M11	3	76	Triode
M12	2	218	Triode

As it is seen through Table 16, the M7 and M8 are in triode region and was concluded one more time that for this region were obtained the best results for gain and noise factor in comparison with the saturation zone.

Gain Simulations at 0.6 V

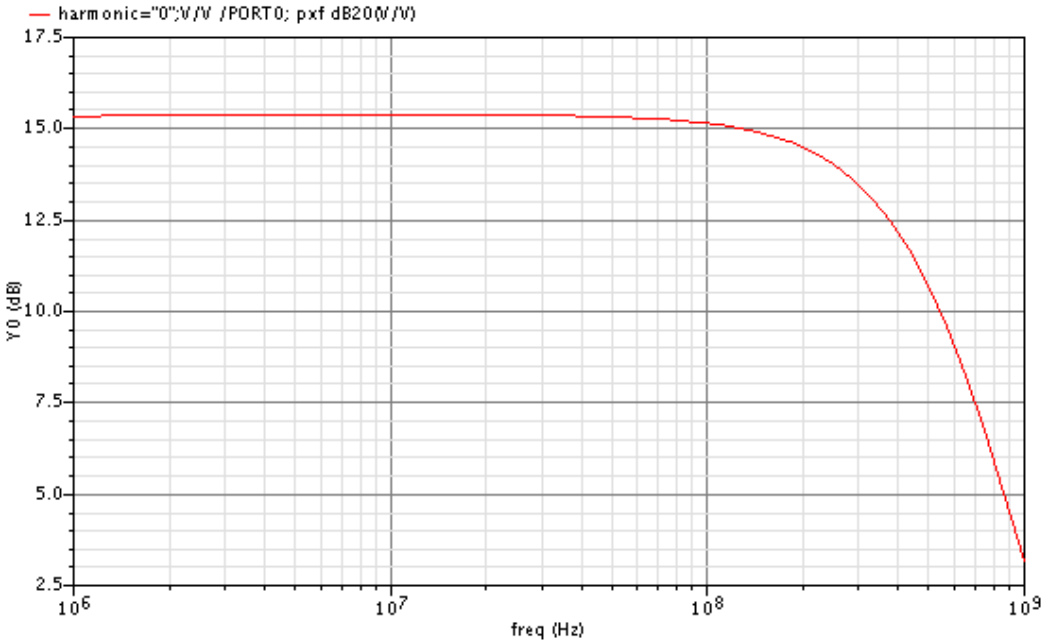


Figure 44-Gain Simulations at 0.6 V.

Noise Factor Simulations at 0.6 V

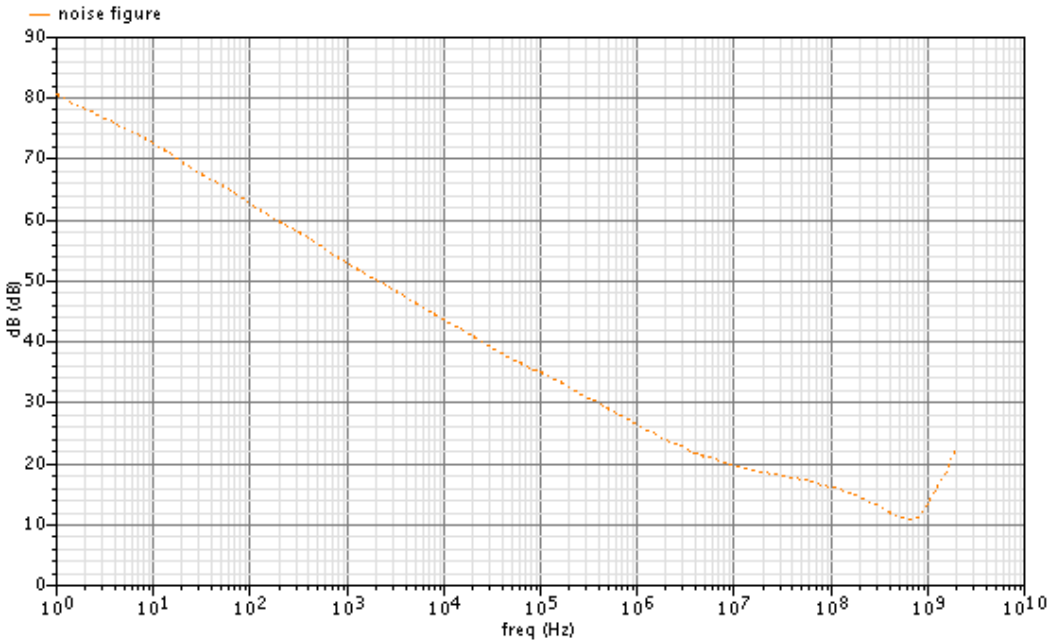


Figure 45-Noise Factor Simulations at 0.6 V.

PVT Variations at 1.2 V

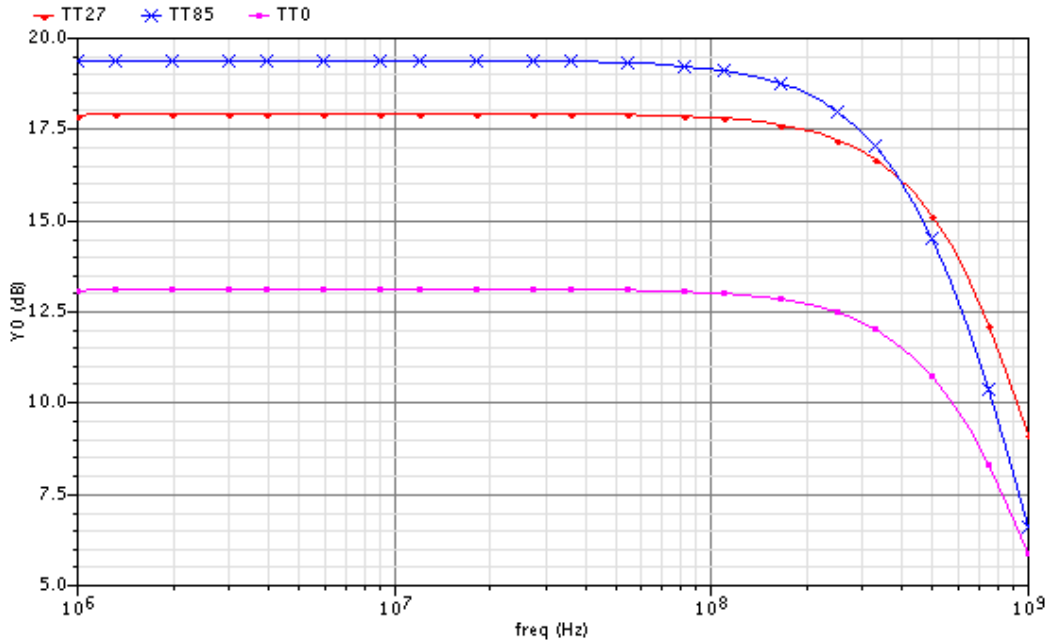


Figure 46-TT Simulations at 1.2 V.

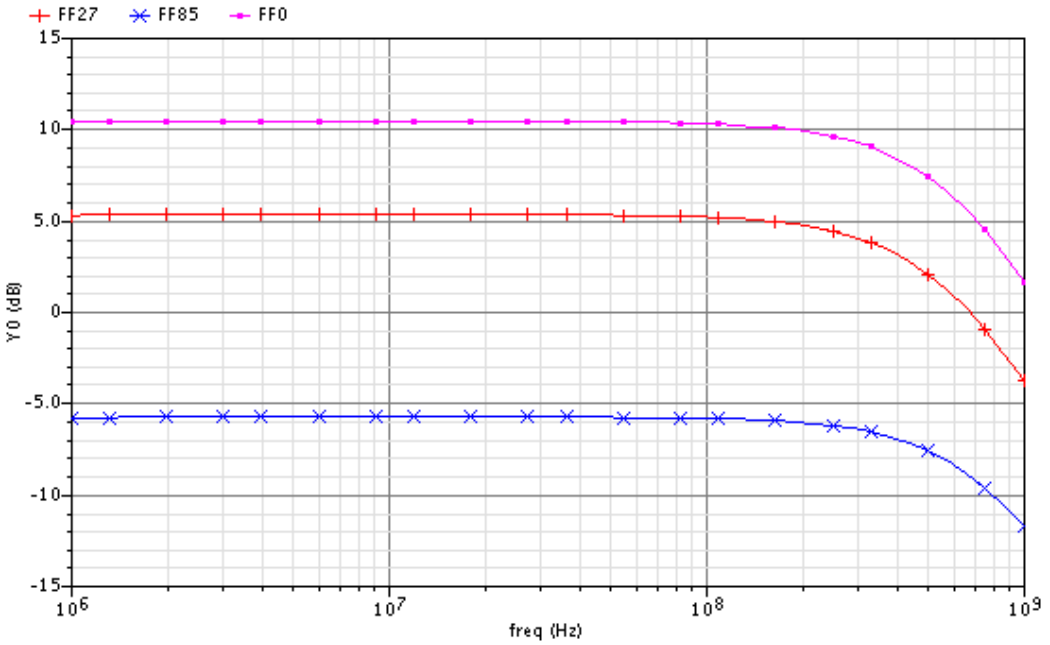


Figure 47-FF Simulations at 1.2 V.

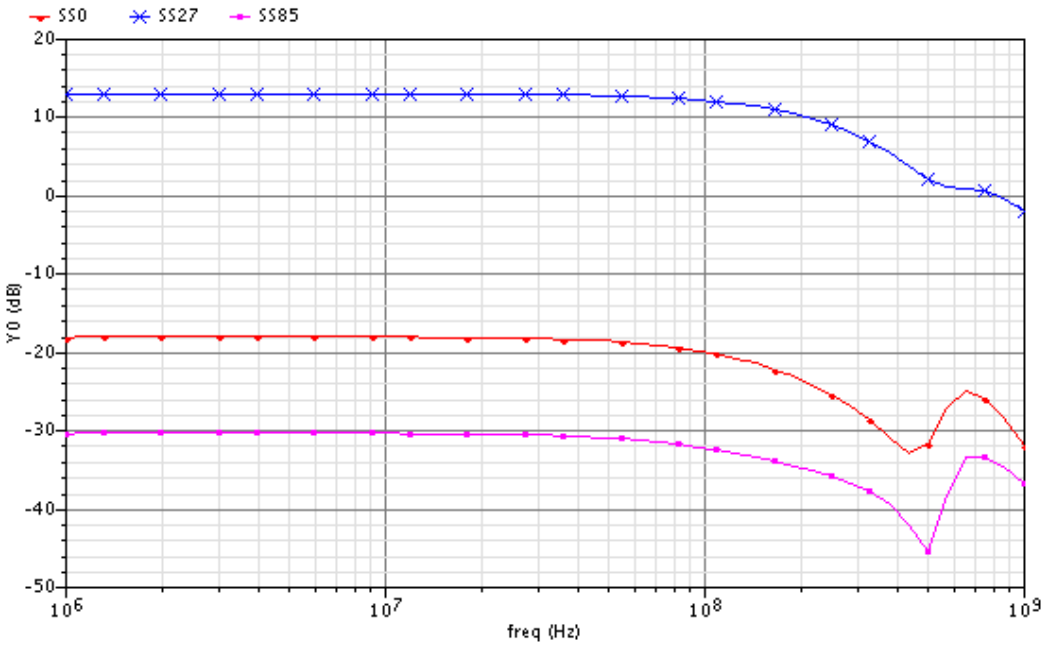


Figure 48-SS Simulations 1.2 V.

PVT at 0.8 V

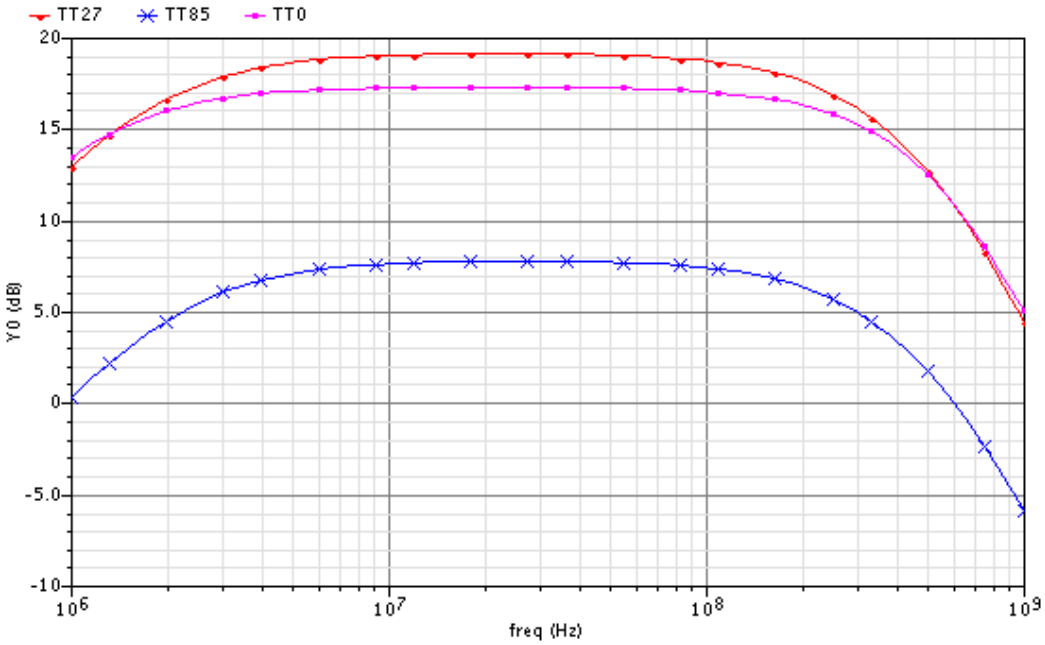


Figure 49- TT Simulations at 0.8 V.

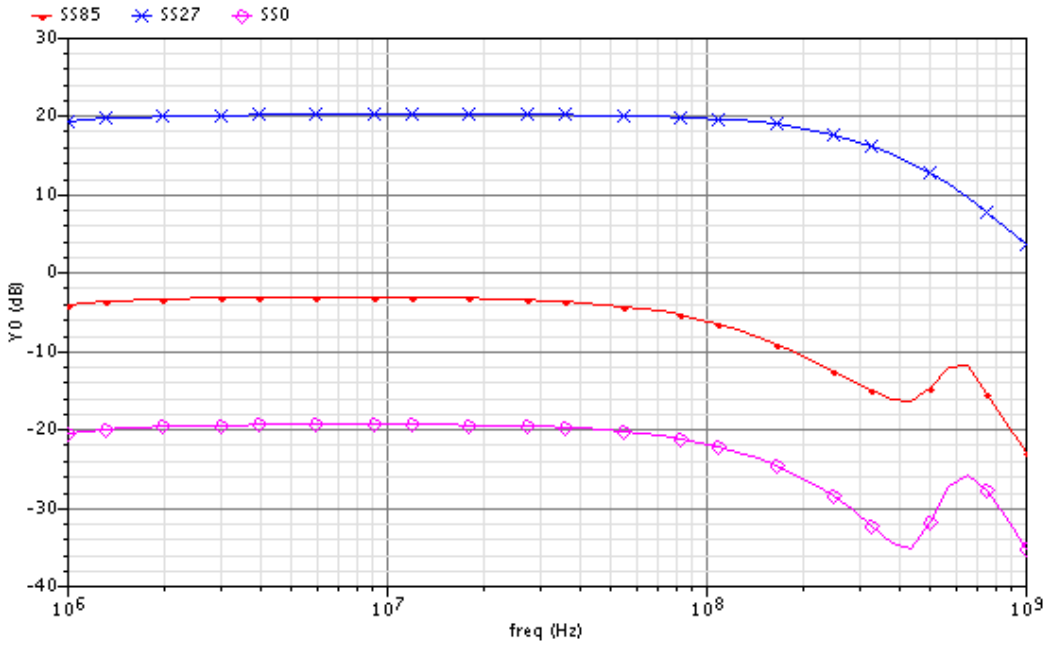


Figure 50-SS Simulations at 0.8 V.

PVT at 0.6 V

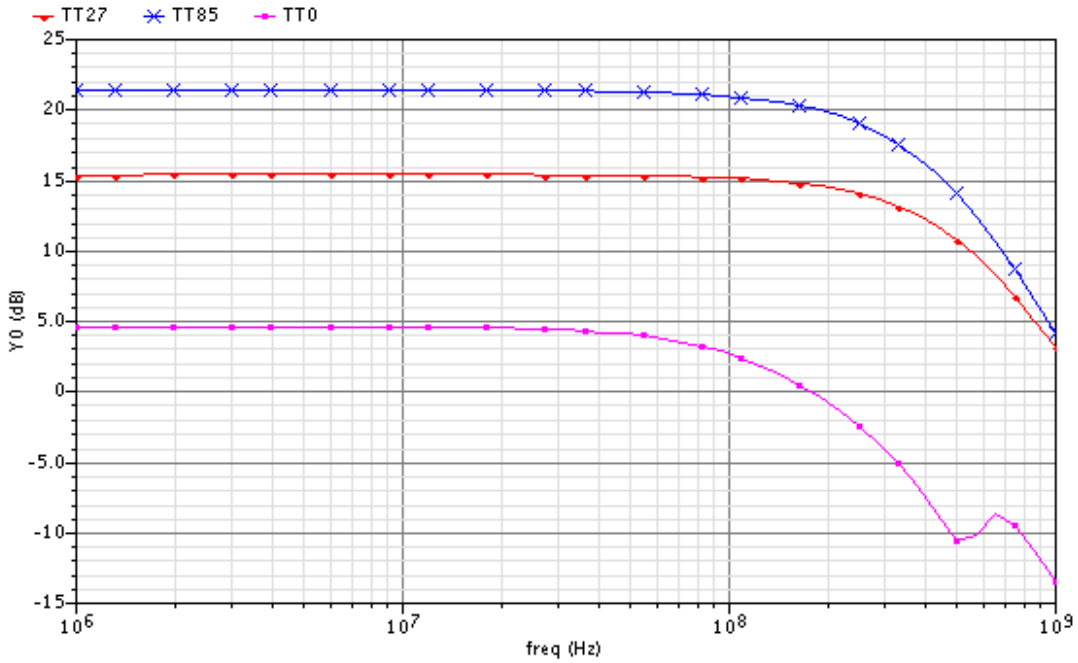


Figure 51-TT Simulations at 0.6 V.

10 MHz	Table 17-Results at 10MHz**.**					
Vdd (V)	AV (dB)	NF (dB)	1 dB Compression	IIP2 (dBm)	IIP3 (dBm)	PDC (m W)
1.2	18	16	-19	-17.8	-18.8	11.85
0.8	18.5	14.5	-28.9	-23.1	-26.2	4.57
0.6	15.5	20	-31	-27.4	-28.6	3.5

Table 18-Models Transistors Results at 1.2 V.

1.2 V	**10 MHz**				
Models	AV(dB)	**Models**	AV(dB)	**Models**	AV(dB)
TT at 0º	13	**FF at 0º**	11.5	**SS at 0º**	12.5
TT at 27º	18	**FF at 27º**	6	**SS at 27º**	-18
TT at 85º	19.5	**FF at 85º**	-6	**SS at 85º**	-30

Table 19-Models Transistors Results at 0.8 V.

0.8 V	**10 MHz**				
Models	AV(dB)	**Models**	AV(dB)	**Models**	AV(dB)
TT at 0º	16	**FF at 0º**	-3.5	**SS at 0º**	-
TT at 27º	19	**FF at 27º**	20	**SS at 27º**	-
TT at 85º	7.5	**FF at 85º**	-20	**SS at 85º**	-

Table 20-Models Transistors Results at 0.6 V.

0.6 V	**10 MHz**				
Models	AV(dB)	**Models**	AV(dB)	**Models**	AV(dB)
TT at 0º	5	**FF at 0º**	-	**SS at 0º**	-
TT at 27º	15.5	**FF at 27º**	-	**SS at 27º**	-
TT at 85º	21.5	**FF at 85º**	-	**SS at 85º**	-

It is seen through the Table 17, 19, 20, 21 and through Figure 40 to Figure 51 above that it were achieved good results for all the supply voltage in general, as well as the main target of this project which is related with low voltage and low consumption. For the gain, the best value was 21.5 dB at 0.6 V with TT models at 85º, for the noise factor the best value was 14.5 dB at 0.8 V with TT models at 27º and for the power the best value was 3.5 mW at 0.6 V.

When the total results are seen, does not make sense refer that this circuit can operate with any models transistors in any circumstances, but in general or in some kind of range the circuit meets the requirements, for example for the TT model between 0.6 and 1.2 V and between 0 and 85º it was obtained an average of 15 dB for the gain. In relation to the all graphs related with the noise factor, it is possible to see the flicker noise at 10 MHz, but this is not a big problem because in a full real receiver would be used some filters able to remove that noise, so this problem can be easily solved. The results related with these simulations are good and all of them are below 20 dB. In relation to the results obtained for the 1 dB compression, IIP2 and IIP3, they are not the best but, were the possible in this configuration, the graphs are not showed due to the large number of simulations that are done in this document.

All circuits are limited and this has also their problems and one of these problems are related with the fact to be possible to work in a range between 0.6-1.2 V with stability but, when simulations are done for example at 0.5 V of supply voltage, the circuit simply collapses even trying doing a total new sizing, which is showed in figure below.

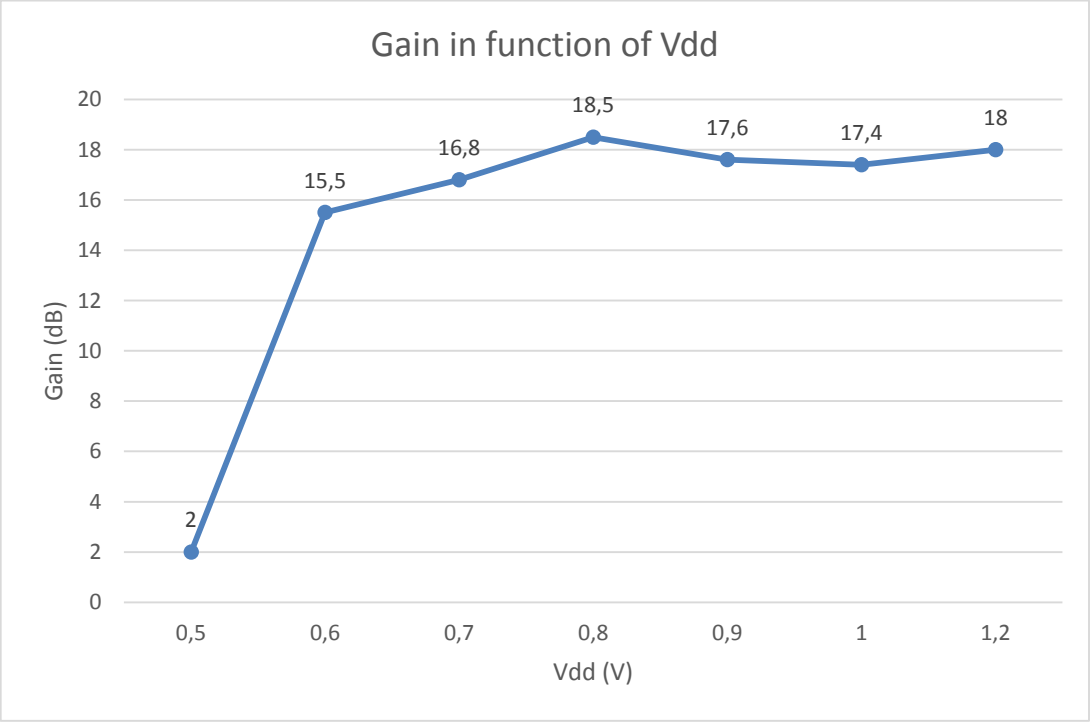


Figure 52-Gain in Function of Vdd.

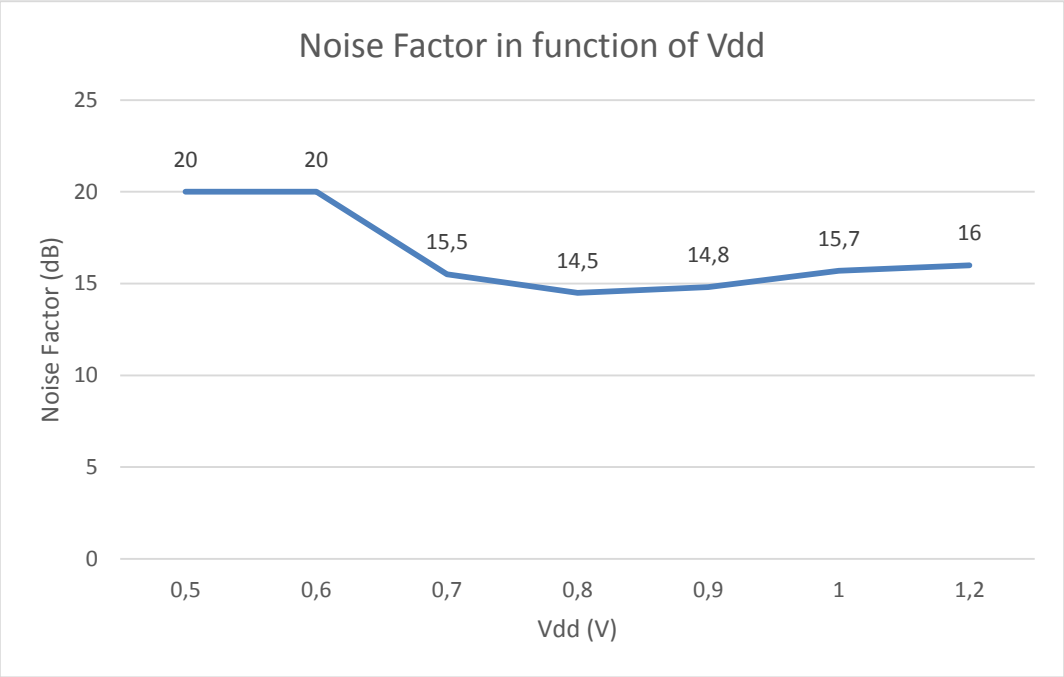


Figure 53-Noise Factor in function of Vdd.

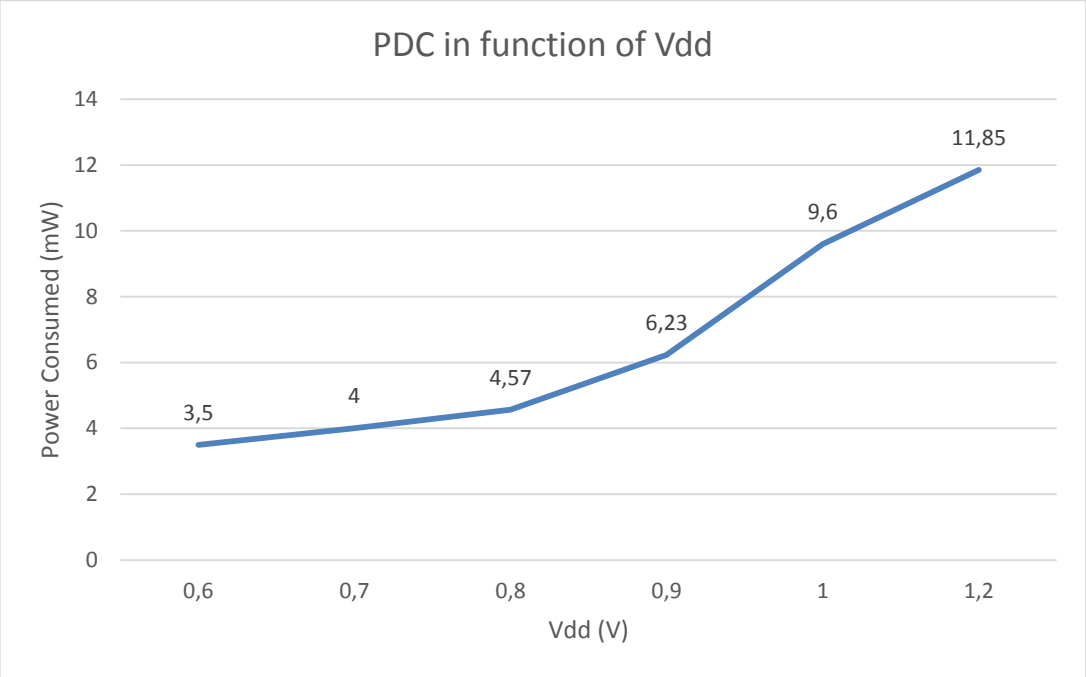


Figure 54-PDC in function of Vdd.

Through Figure 52, Figure 53 and Figure 54 above it is possible to note that the best performance is situated at 0.8 V in relation to the others supply voltages with 18.5 dB of gain, 14.5 dB of noise factor and 4.57 mW of power consumed.

Chapter 6

Conclusion and Future Work

The main goal of this thesis that is related with the development of a LM operating at low voltage and low consumption was perfectly fulfilled. Obviously that none project is perfect and this has also their problems and limitations, but in general the duty was accomplished. Speaking specifically about the work, and beginning by the LNA, it is possible to say that there were not any problems to achieve the low voltage, were used DTMOS in four transistors which were crucial to the each premature saturation at low voltage values.

The resistors in traditional balun were replaced by two transistors in triode region, which allowed less distortion and consequently in this case more gain and less noise factor. In both gate of these transistors were connected voltage controllers that allow each polarization and consequently the increasing of V_{DSAT}. These two voltage blocks and a current source were crucial to guarantee the balance of each stage which allowed the increase of gain.

The sizing was not difficult and the best gain and noise factor values registered in TT conditions were precisely 19.3 and 2.26 dB at 1.2 V, nevertheless the circuit is available to operate in a range between 0.6 and 1.2 V. The study and correspondent sizing of Mixer was more difficult due to the simple structure, but one more time DTMOS and voltage controllers were crucial to the low voltage, and if in the beginning this Mixer didn't has gain and the noise factor values close to 30 and 40 dB, in the present moment at 1.2 V it were achieved due to these techniques 2.3 dB for the gain and approximately 23 dB for the noise factor.

When the two circuits were connected, there were some problems associated with the DC value between them, because the same value when they were divided it was not the same, thus to solve that issue, it was placed a voltage controller with the objective to tune that value and achieve the best for the gain. Instead of an ideal source, it could be used some transistors which would have the same application but due to the fact of this circuit does not be produced it was not necessary. Not so important such as low voltage or low consumption for this thesis, obviously would be interesting to verify if this system would be capable to operate with others models of transistors and in extreme conditions at 0 and 85º. It was verified some good values, for example at 1.2 V to TT85º 19.5 dB, to TT0º at 0.8 V 16dB, to FF27º at 0.8 V 20dB, and to TT85º at 0.6 V 21.5 dB. As minor goal, these values are quite good and naturally would be necessary others techniques or possibly a new sizing.

Chapter 6. Conclusion and Future Work

It is also crucial to make a reference to the results achieved, comparing the proposed balun LNA with the balun LNA that was studied in the subject Electronic 4, which served the reference to this thesis and with others works related with the theme.

Table 21- Balun LNA VS Proposed LNA.

	BW (GHz)	**Av (dB)**	**NF (dB)**	**IIP2 (dBm)**	**IIP3 (dBm)**	**PDC (mW)**	**FOM (mW^{-1})**
Balun LNA	0.4-0.9	10.5	<3.3	15.3	-3.9	9.5	0.32
Proposed LNA	0.4-0.9	19.3	<2.3	-11.2	-12.2	11.8	1.15

It is possible to note through Table 21 that was achieved a boost of 9 dB for the gain and the noise factor was reduced in 1dB. Others comments could be done, when are compared results of this work at 1.2 and 0.6 V for the gain, noise factor and consumption with others works. It is fair to note that these projects were not done with the same technology, but the range frequency and the applications were the same and, it is seen through Table 22 that even this work at 0.6 V achieved better results than [22, 23] at 1.8 V, more gain in more or less 2dB, less noise factor in 2dB and less consumption in 6mW.

Table 22-Performance Proposed LNA VS Others

	Tech (nm)	**Band (GHz)**	**Av (dB)**	**NF (dB)**	**PDC (mW)**	**FOM (mW^{-1})**
This work at 1.2 V	130	0.4-0.9	19.3	<2.3	11.8	1.15
This work at 0.6 V	130	0.4-0.9	17.2	<2.6	4	2.14
[22]*	180	0.1-0.9	15	<4.2	10	0.3
[23]*	180	0.5-0.9	16	<4.3	22	0.2

Chapter 6. Conclusion and Future Work

It is also interesting to prove de veracity between theoretical and practical results related with the gain for the LNA and the Mixer.

Table 23-Theoretical and Pratical results

At 1.2 V		
Circuit	AV(Practical)	AV(Theoretical)
LNA	19.3	18.6
MIXER	2.3	2

For future work in a PhD, it would be important to highlight some important points to truly complement this project.

First stage

- Development of a full receiver at 1.2 V.
- Improve the performance at TT, FF and SS models transistors.

Second stage

- Development of a full receiver at 0.6 V.
- Improve the performance of the system to be possible operate at 0.5 or 0.4 V.
- Make the Layout.

Bibliography

[1] B. Razavi, "*RF Microelectronics"*. Prentice-Hall, 1998.

[2] J. Crols and M.Steyaert, "*CMOS Wireless Transceiver Design*", Kluwer, 1997.

[3] T. H. Lee, *The Design of CMOS Radio Frequency Integrated Circuits (2nd edition)*. Cambridge University Press, 2004.

[4] A. S. Sedra, K.C. Smith, "*Microelectronics Circuits*", Oxford University Press, 1997.

[5] David A. Johns and Ken Martin, "*Analog Integrated Circuit Design*", John Wiley & Sons, 1997.

[6] Manuel de Medeiros Silva, "*Introdução aos Circuitos Elétricos e Eletrónicos*", Fundação Calouste Gulbenkian (Book in Portuguese Language), 2nd edition, 2001.

[7] Manuel de Medeiros Silva, "*Circuitos com Transístores Bipolares e MOS*", Fundação Calouste Gulbenkian (Book in Portuguese language).

[8] Fariborz Assederaghi, Member, IEEE, Dennis Sinitsky, Septhen A.Parke,Jeffrey Bokor, Ping K.Ko, Fellow, IEEE, and Chenming Hu, Fellow, IEEE , "*Dynamic Threshold- Voltage MOSFET (DTMOS) for Ultra- Low Voltage VLSI*" Electron. Lett, vol 38, no. 22,pp. 1362-1364, Oct. 2002.

[9] S. Blaakmeer, E. Klumperink, D. Leenaerts, and B. Nauta, "*Wideband Balun-LNA with Simultaneous Outputs Balancing, Noise-Canceling and Distortion-Canceling*", *IEEE J. Solid-State Circuits*, vol. 43, no. 6,pp. 1341-1350, June 2008.

[10] K.W. Chew, K.S. Yeo, and S. F. Chu, "*Effect of technology scaling on the 1/f noise of deep submicron MOS transistors*", *Solid-State Electron*, vol. 48, pp. 1101-1109, 2004.

[11] M. Manghisoni, L. Ratti, V.Re ,V.Speziali and G.Traversi, "*Noise Characterization of 130 nm and 90 nm CMOS Technologies for Analo Front-end Electronics*", *IEEE Nuclear Science Symposium Conference*,vol.1, pp. 214 – 218, 2006.

[12] M. Mudrow, W. Wanalertak and L. Forbes, "Thermal Noise Limits in Nanoscale Electronics", Microelectronics and Electron Devices, 2006.WMED '06.2006 IEEE Workshop on

[13] Rui Santos-Tavares, Edinei Santin, Rui Borrego, João Oliveira, João Goes, "Gain Enhancement and Input Parasitic Capacitance Reduction of a Single-Stage OTAs by using Differential Voltage Combiners", *MIXDES conference 2013*.

[14] F. Leyn, W. Daems, G. Gielen, W. Sansen, "A behavioral signal path modeling methodology for qualitative insight in and efficient sizing of CMOS opamps", CAD, Dig. of Tech. Papers, pp. 374-381, Nov 1997.

[15] Rui Borrego, João Oliveira, João Goes, " A 2.3-dB NF CMOS Low Voltage LNA Optimized for Medical Applications at 600MHz", *MIXDES conference 2013*.

[16] J. Ferreira, I. Bastos, L. Oliveira, J. Oliveira, T. Michalak, P. Pankiewicz, B. Nowacki, P. Makosa, and A. Rybarczyk, "Lna, oscillator and mixer co-design for compact rfcmos ism receivers," *Mixed Design of Integrated Circuits Systems*, 2009. *MIXDES'09.MIXDES-16th International Conference*, pp. 291_295, jun 2009.

[17] I. Bastos, L.B. Oliveira, J. Goes, M. Silva, "Balun LNA with continuously controllable gain and with noise and distortion cancellation" *IEEE Int. Symposium Circuit and Systems (ISCAS 2012)*, pp. 2143 - 2146, May 2012.

[18] S. C. Blaakmeer, E. A. M. Klumperink, D. M. W. Leenaerts, and B. Nauta, _Wideband balun-lna with simultaneous output balancing, noise-canceling and distortioncanceling,_ IEEE J.Solid-State Circuits, vol. 43, no. 6, jun 2008.

[19] Sanming Hu, Yong-Zhong Xiong, Lei Wang, and Bo Zhang, "A 135GHz Single-Ended Mixer in 0.13μm SiGe HBT for High-Speed Demodulation", 2012 IEEE International Symposium on Radio-Frequency Integration Technology (RFIT).

[20] Jie Long, and Robert J.Weber, "A Integrated 2.4GHz CMOS RF Front-End", in Proc. IEEE AerospaceConf., vol. 4, pp. 2378-2383, 2004.

[21] Henrik Sjoland, Sven Mattisson,"A 100-MHz CMOS Wide-Band IF Amplifier", IEEE JOURNAL OF SOLID-STATE CIRCUITS, VOL. 33, NO. 4, APRIL 1998.

[22] K. Han; L. Zou; Y. Liao; H. Min; Z. Tang; , "A wideband CMOS variable gain low noise amplifier based on single-to-differential stage for TV tuner applications," *IEEE Solid-State Circuits Conference, A-SSCC '08*, pp.457-460, 3-5 Nov. 2008.

[23] J. Xiao, I. Mehr, J. Silva-Martinez, "A High Dynamic Range CMOS Variable Gain Amplifier for Mobile DTV Tuner," *IEEE J. Solid-State Circuits*, vol.42, no.2, pp.292-301, Feb. 2007.

Appendix A

CMOS Basic Information

The first step which is mandatory to do, when an electronic thesis is written related with CMOS technology, it is speak about the main aspects that can determine if that thesis has been done with sense and knowledge. These aspects are very important, but for the expert or the common lector understand them in this chapter are essential for the global understanding of this document posteriorly.

NMOS and PMOS Transistors:

In electronic and in this case CMOS technology, NMOS and PMOS transistors are crucial in any circuit used for electronic or telecommunication applications. These components allow a lot of changes in a circuit and changing for example them size it is possible, to increase or decrease de gain, increase or decrease de NF and obtain a better IP2 or IP3,so the performance of each circuits depends a lot of them. First of all, these transistors are commonly represented as in Figure 55 [1] and Figure 56 [1].

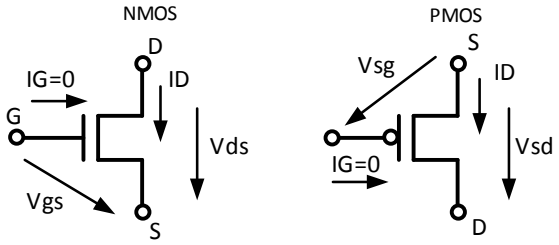


Figure 55-NMOS and PMOS Transistors.

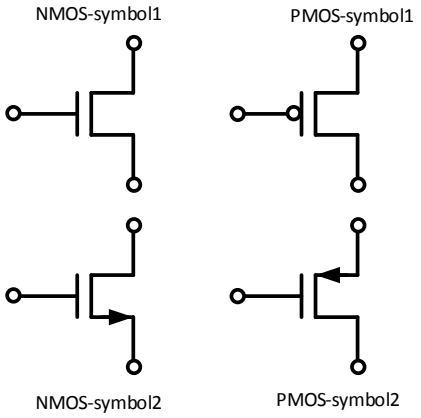


Figure 56-NMOS and PMOS Transistors.

Modes of operation:

Both types of transistors have them work regions and in general exist six such as: cut-off, weak inversion, strong inversion, linear region, triode region and finally active region. These work regions are valid for NMOS and PMOS, it is only mandatory to have in attention that source and drain are exchanged [4, 5, 6, 7].

Cut-off and Weak-Inversion:

In this case, the analyses are done based on figures $I_D - V_{GS}$ as it is seen in Figure 57 [1] and the transistor is in the cut-off region, for negatives gate voltages when the drain and the bulk form a reversed biased p-n junction, with equation 1 [1]:

$$\begin{cases} V_S = V_B \\ V_{GS} \leq 0 \end{cases} \Rightarrow I_D = 0 \quad \textbf{(1)}$$

For very small positive gates smaller than V_{Tn} , very small proportions of current can flow, but for a question of simplify, it is considered that the transistor have some drain current, $I_D \approx 0$ and it has a similar behave like a bipolar transistor, with equation 2 [1]:

$$I_D \approx I_S . e^{\frac{V_{GS}}{V_T}} \quad \textbf{(2)}$$

Where I_S and V_T represent the limit weak inversion current which is proportional to $\frac{W}{L}$ and the thermal noise $\frac{KT}{q}$. This region is very interesting to refer, when applications are related with biomedical circuits for example where it is worked with low frequencies.

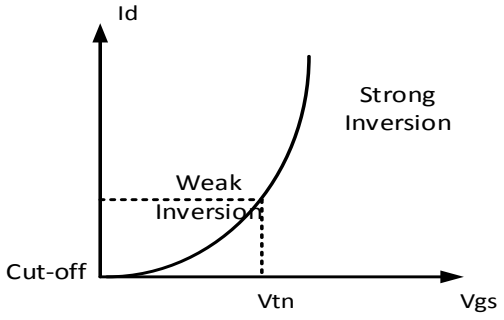


Figure 57-Modes of Operation.

Linear and Triode regions:

When V_{GS} is bigger than V_{Tn}, the transistor is said that is in moderate/strong inversion. In this situation the drain current becomes positive and proportional to $(V_{GS} - V_{Tn})$ and V_{DS} is positive but very small as it is seen in Figure 58 [1]. This region is called the linear region and the transistor behaves like a resistor and in this case V_{DS} is lesser thanV_{DSAT} with equation 3 [1].

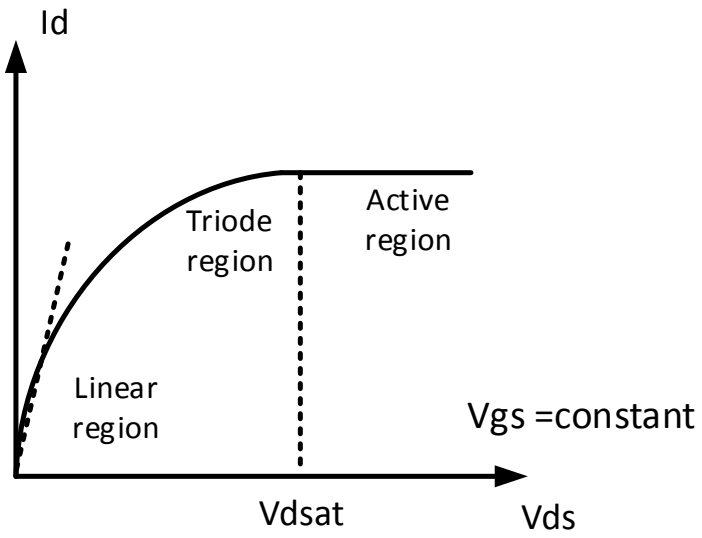


Figure 58-Modes of Operation.

$$\begin{cases} V_{GS} > V_{Tn} \\ 0 < V_{DS} \ll 1 \end{cases} \Rightarrow I_D = K_n . \frac{W}{L} . (V_{GS} - V_{Tn}) . V_{DS} \quad \textbf{(3)}$$

For larger drain-source voltages, but smaller than the overdrive-voltage the potential of the channel is increase and the expression becomes more complex in the triode region [4, 5, 6, 7]. For this situation, V_{DS} remains lesser than V_{DSAT} but the value is bigger in relation with linear region. In these cases the analyses are done based on $I_D - V_{DS}$ with equation 4 [1].

$$\begin{cases} V_{GS} > V_{Tn} \\ 0 < V_{DS} < (V_{GS} - V_{Tn}) \end{cases} \Rightarrow I_D = K_n . \frac{W}{L} . \left[(V_{GS} - V_{Tn}) . V_{DS} - \frac{V_{DS}^2}{2} \right] \quad \textbf{(4)}$$

Saturation region:

A transistor is biased in the saturation region when his drain-source voltage is larger than overdrive voltage, in other words: $V_{DS} > (V_{GS} - V_{Tn})$. This is the reason why the part $(V_{GS} - V_{Tn})$ is called V_{DSAT} with equation 5 [1].

(5)

$$\begin{cases} V_{GS} > V_{Tn} \\ V_{DSAT} = (V_{GS} - V_{Tn}) \Rightarrow I_D = \frac{K_n}{2} . \frac{W}{L} . (V_{GS} - V_{Tn})^2 \\ V_{DS} > V_{DSAT} \end{cases}$$

In general in electronic circuits, transistors work in saturation or active region, to be possible obtain more gain and stability, but sometimes if it is referred about 2 stage amplifier could be more efficient to get better results working with them in triode region [4, 5, 6, 7].

It is also important to note that, due to the fact of K_n be $\frac{1}{3}$ of K_n makes the PMOS slower three times than NMOS. This note is crucial also to make a good study of them and in this graph exists an ideal point situated between triode and active region where is the best point for the best performances of a CMOS transistor, but this theme is in discussion yet.

Body effect:

Another theme important to referrer it is the body effect, in general all equations assume that the source of a NMOS component is connected with bulk and this on the other hand is connected with the most negative voltage. Although, often the source and bulk can be at different voltage potentials such as the gate when it is required to work with DTMOS for example. In these situations the threshold voltage,V_{Tn}, and the source-bulk voltage, V_{SB} increase too.

Gain

When it is spoken about gain in electronic devices such as amplifiers, buffers, LNA's and mixers for example, this gain is something that can available them quality. In other words how much bigger could be this parameter, better will be the capacity to amplify the signal. This is crucial because GPS, cell phone or simply antennas need gain to receive and send data. In CMOS technology it is mandatory to refer at least three important types of gain, one of them are: power gain, voltage gain and conversion gain. Power gain and voltage gain are related with LNA's, if the analyses are done with s-parameters it is spoken about power gain but, if the analyses are done with transient it is spoken about voltage gain. Conversion gain is used for mixers and is related with the work frequency of LNA and with the work frequency of oscillators. This is a general explanation because more details specifically are explained posteriorly in this document.

Noise

When it is referred about Noise, it is any undesired signal that is added to the desired signal, several experts referred it like a kind of "electronic garbage" and the main goal is try to maximize the signal to Noise ratio. In general Noise can be divided in two categories:

- Deterministic Noise:
  This kind of Noise is related with interference caused by others signals, it can be easily reduced by minimizing the coupling of undesired signals.

- Random Noise:
  This kind of Noise is related with random effects and it is presented at a fundamental level in most electronic components, it is possible to be reduced doing a careful circuit design.

These notions are important to understand globally which means the Noise, but specifically it is more appropriate to refer several kinds of Noise and those are more referred in several electronic documents such as Flicker Noise and Thermal Noise, although exist others three common like Shot noise, Burst noise and Avalanche noise.

Flicker Noise

This kind of Noise as it is seen graphically in Figure 59 [1] and in Figure 60 [1], it is normally associated with impurity atoms in the semiconductor crystal and these, create energy states that trap and done the carriers. In general speaking about the impact of it in transistors, PMOS transistors have less flicker noise than NMOS and this action can be related with the fact that NMOS are faster than PMOS, if the physical size of the transistor increases the corresponding flicker noise decreases.

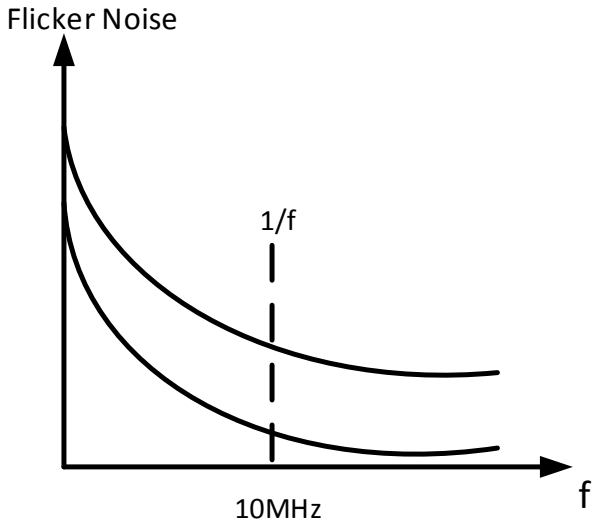


Figure 59-Flicker Noise.

The power spectral density is given by equation 6:

$$S_{vf} = \frac{K}{C_{ox} * W * L} * \frac{1}{f} \quad \textbf{(6)}$$

This equation is crucial to understand how varies the spectral density in a bandwidth range and that it represents an area.

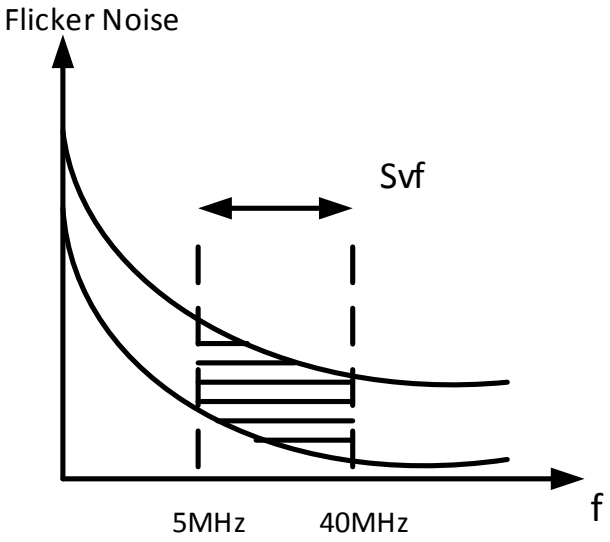


Figure 60-Flicker Noise.

Thermal Noise

This kind of noise was experimentally demonstrated by Johnson in 1926 and theoretically derives by Nyquist in 1928. It is related with thermal fluctuations in the electron density within a conductor. This fluctuation of electric charges exists in all conductors producing a random variation of potential between the ends of the conductor. The electric charges are found to be in a state of thermal agitation in thermodynamic equilibrium with the heat motion of the atoms of the conductor [1, 12].

1 dB Compression Point

This theme it is fundamental to understand the general behavior of circuits and consequently the transistor. When a receiver in this case is developed and optimized, it is not only crucial to achieve in gain and noise factor good results, but also it is mandatory to achieve good results in this kind of simulations because the linearity prove or not the reliability of the global system [1]. The 1 dB gain compression point is defined as the power gain, where the nonlinearities of the transistor reduce the power gain by 1 dB over the small-signal power gain as it is seen in Figure 61 [1]. It is important to note that how much bigger this value is, better is for example the LNA or the Mixer.

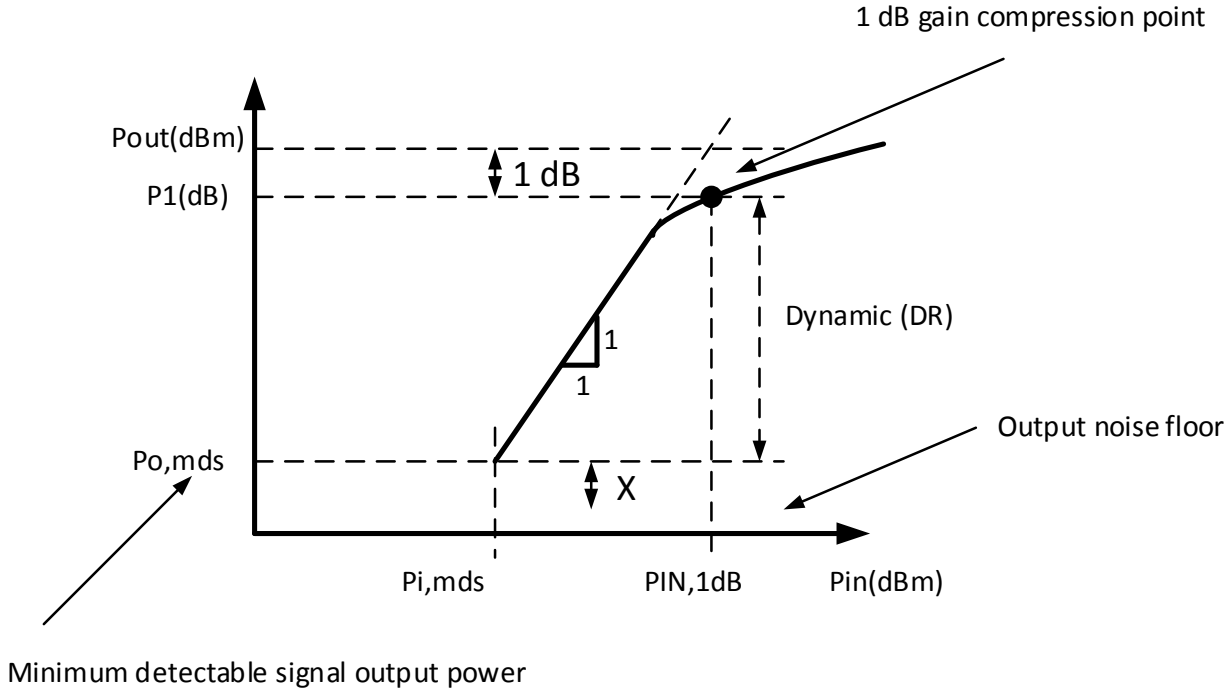


Figure 61-1 dB Gain Compression Point.

To express better the content of the graph some equations are important to understand it with equation 7:

$$G_{1dB}(dB) = G_0(dB) - 1$$

$$G_{1dB}(dB) = \frac{P_{1dB}}{P_{IN,1dB}} \qquad P_{1dB}(dBm) = P_{IN,1dB}(dBm) + G_{1dB}(dB)$$

$$DR = P_{1dB} - P_{0,mds} \quad (dB)$$

$$P_{0,mds}(dBm) = P_{i,mds}(dBm) + G_A(dB)$$

$$P_{0,mds}(dBm) = -174dBm + 10logB + F(dB) + X(dB) + G_A(dB) \qquad \textbf{(7)}$$

Where $G_{1dB}(dB)$ represents the small signal power gain, DR the dynamic range, $-174dBm + 10logB$ the noise power in B, $F(dB)$ the amplifier noise figure, $X(dB)$ the detection margin 3 dB and $G_A(dB)$ the available gain.

Harmonic Distortion and Intermodulation

One of the most important aspects when some thesis or project is related with receivers, which include in your extension blocks such as LNA's and Mixers, it is the harmonic distortion more specifically the IP2 and IP3. There are some points that can characterize IP2 and IP3, for example in the first:

1. Component DC
2. 2nd harmonic:2f1 and 2f2
3. 2nd order intermodulation products:f1±f2

And in the second:

1. f1 and f2
2. 3rd harmonic:3f1 and 3f2
3. 3rd order intermodulation products:2f1±f2 and 2f1±f2

Applying two sinusoidal frequencies to the amplifier that it is showed in Figure 62:

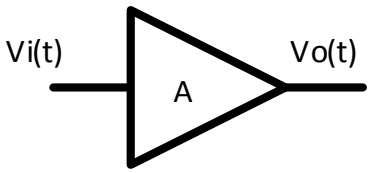


Figure 62-Ampop.

$$V_i(t) = cos(2\pi f1t) + cos(2\pi f2t) \quad \textbf{(8)}$$

$$V_O(t) = AV_i(t) + BV_i^2(t) + CV_i^3(t) \quad \textbf{(9)}$$

The first and second parcel corresponds to the IP2 and the third correspond to the IP3 and, a source of distortion in amplifier is that caused by intermodulation products. The frequencies that are used to make the simulations of IP2 and IP3 on the software that is used, for example to the LNA are the work frequency that in this thesis is 600MHz and another frequency which can be 400 or 800MHz.The input and output frequencies are shown in Figure 63 [1] and Figure 64 [1].

Input frequencies:

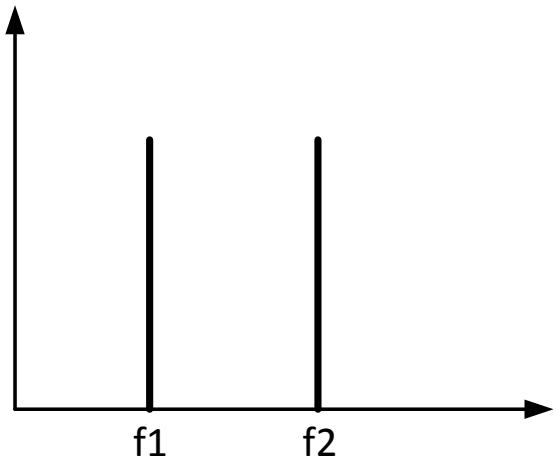


Figure 63-Input Frequencies.

Output frequencies:

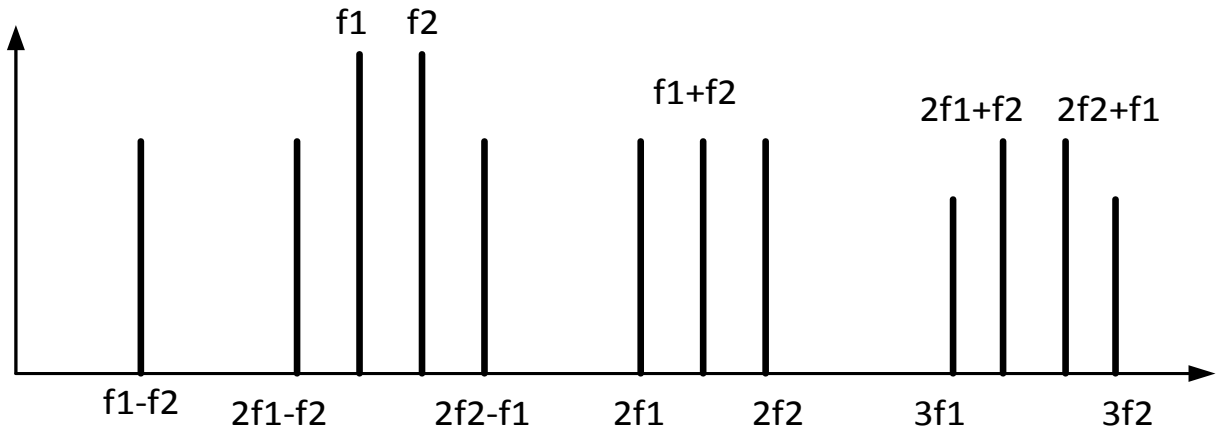


Figure 64-Output Frequencies.

CMOS Common-Source Stage

Common-Source amplifier is one of the basic single-stage amplifiers, and in this case it is possible to note in Figure 64 [1] that the current source that provides the drain current to the NMOS transistor M is usually done by a current-mirror active load. In this topology the input ac signal V_{in} is connected to the gate transistor and the output V_{out} is connected to the drain. All dc supply and bias voltage are short-circuited to the ground and all dc currents are replaced by open circuits when is required to make the small-signals equivalent circuit [4, 5, 6, 7].

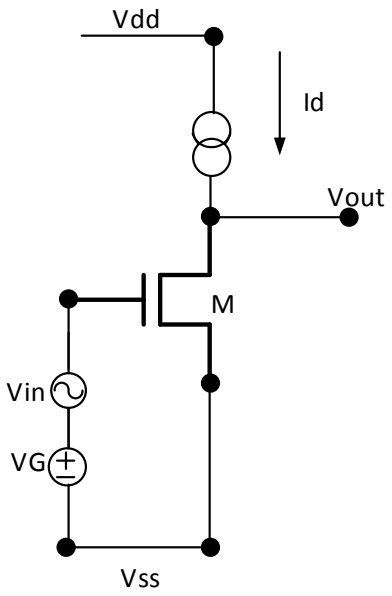


Figure 65-Common Source Circuit.

Doing a short analyze for this circuit and calculating several parameters such as: gain, input impedance and output impedance, it is obtained the follow group of equations through Figure 66 [1]).

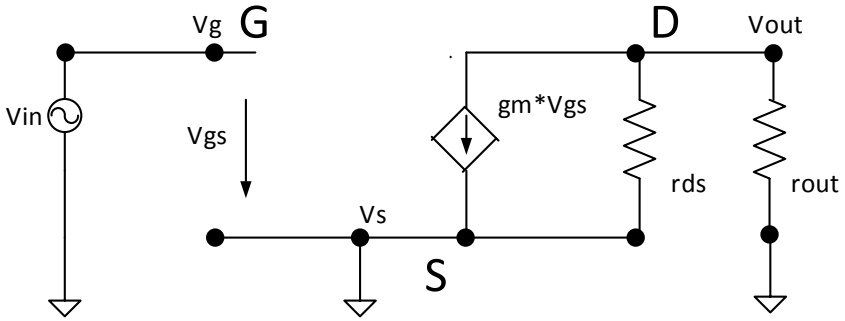


Figure 66-Common Source Small Signals.

Using the small-signals analyses it is possible to obtain the gain and for this case $\boldsymbol{V_{in} = V_{GS}}$, therefore the voltage gain is given by equation 10 [1].

$$A_V = \frac{V_{out}}{V_{in}} = \frac{-gm * (r_{ds}||r_{out}) * V_{GS}}{V_{GS}} = -g_m * (r_{ds}||r_{out}) = \frac{-g_m}{g_{ds} + g_{out}} \quad \textbf{(10)}$$

where, $\boldsymbol{g_{ds}}$ and $\boldsymbol{g_{out}}$ represent the drain-source conductance and the output conductance. Usually the typical gain has a range value between -10 and -100 depend the size of transistor, drain source and the technology used. The input impedance of this circuit is given by equation 11 [1]:

$$R_{in} = \frac{V_{in}}{i_{in}} = \infty \quad \textbf{(11)}$$

The output impedance is given by equation 12 [1]:

$$R_{out} = \frac{V_{out}}{i_{out}} = (r_{ds}||r_{out}) \quad \textbf{(12)}$$

This value can be very high and can range from some tens of kΩ to a few hundreds kΩ, depending on the drain current.

CMOS Common-Gate Stage

The second basic single-stage amplifier is the common-gate amplifier shown in Figure 67 [1]. In this case the input ac signal V_{in}, is connected to the source of the transistor and the V_{out} is connected with at it is drain. Once again the NMOS is replaced by his small-signal equivalent model and all dc sources are nulled [4, 5, 6, 7].Using the same short-signal analyze like was done for common-source and neglecting the body effect of the transistor the following analyze can be done through Figure 68 [1].

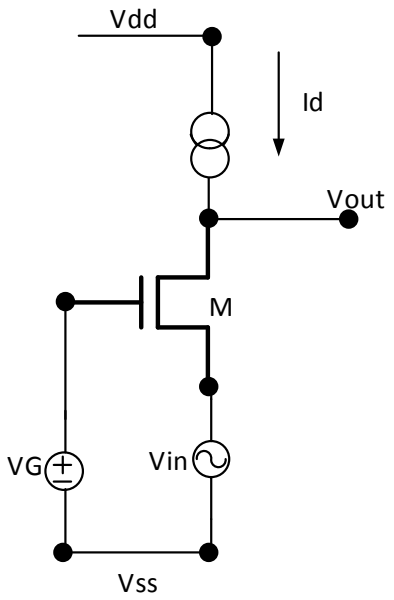


Figure 67-Common Gate Circuit.

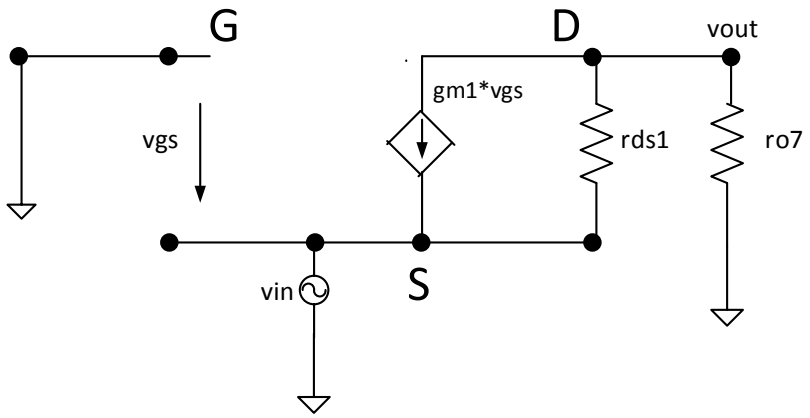


Figure 68-Common Gate Small Signals.

Using the small-signals analyses it is possible to obtain the gain and for this case $\boldsymbol{V_{GS} = -V_{in}}$ therefore the voltage gain is given by:

$$\frac{V_{out}}{r_{out}} + \frac{V_{out} - V_{in}}{r_{ds}} - g_m * V_{in} = 0 \iff g_{out} * V_{out} + g_{ds} * (V_{out} - V_{in}) - g_m * V_{in} = 0$$

with, $g_m \gg \frac{1}{r_{ds}}$ and $g_m \gg \frac{1}{r_{out}}$

The gain is given by equation 13 [1]:

$$A_V = \frac{V_{out}}{V_{in}} = g_m * (r_{ds}||r_{out}) = \frac{g_m}{g_{ds} + g_{out}} \quad \textbf{(13)}$$

Usually the typical gain has a range value between 10 and 100 depend the size of transistor, drain source and the technology used. The input impedance of this circuit is given by equation 14 [1]:

$$R_{in} = \frac{V_{in}}{i_{in}} \approx \frac{1}{g_m} * \left(1 + \frac{r_{out}}{r_{ds}}\right) \quad \textbf{(14)}$$

The output impedance of this circuit is given by equation 15 [1]:

$$R_{out} = \frac{V_{out}}{i_{out}} = (r_{ds}||r_{out}) \quad \textbf{(15)}$$

This is very similar to the common-source amplifier.

2.5 CMOS Common-Drain Stage

The third basic single-stage amplifier is the common-drain amplifier shown in Figure 69 [1] .The input ac signal, V_{in}, is connected to the gate of the transistor and the output V_{out} is connected with at his source. Once again the NMOS is replaced by his small-signal equivalent model and all dc sources are nulled [4, 5, 6, 7]. Again the resistor rout represents the finite output impedance of the biasing current-source, and neglecting the body-effect and writing the nodal equation at the output node with $V_{GS} = (V_{in} - V_{out})$ it will have some differences in the calculus of gain.

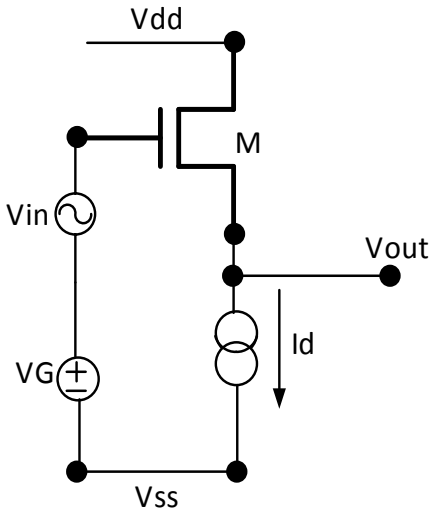


Figure 69-Common Drain Circuit.

$$V_{out} * (g_{ds} + g_{out}) - g_m * (V_{in} - V_{out}) = 0$$

with , $g_m \gg \frac{1}{r_{ds}}$ and $g_m \gg \frac{1}{r_{out}}$

Using the small-signals analyses, it is possible to obtain the gain through Figure 70 [1].

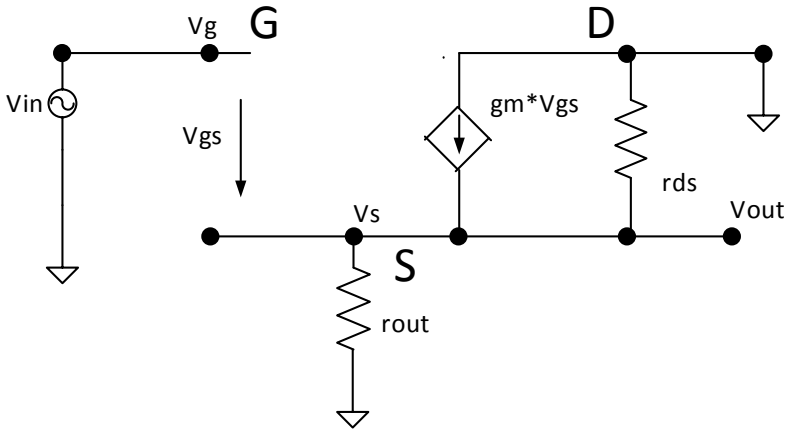


Figure 70.Common Drain Small Signals.

$$A_V = \frac{V_{out}}{V_{in}} = \frac{g_m}{g_m + g_{ds} + g_{out}} \approx 1 \quad \textbf{(16)}$$

The input impedance of this circuit is given by equation 17 [1]:

$$R_{in} = \frac{V_{in}}{i_{in}} = \infty \tag{17}$$

The output impedance of this circuit is given by equation 18 [1]:

$$R_{out} = \frac{V_{out}}{i_{out}} \approx \left(\frac{1}{gm}\right) \tag{18}$$

In the Table 24 [1]**,** it is possible to observe the general characteristics related with the three topologies:

Table 24-Configuration characteristics.

Configuration	Voltage Gain	Input Impedance	Output Impedance
Common-source	$\approx -g_m * (r_{ds} \| \| r_{out})$	High	High
Common-gate	$\approx g_m * (r_{ds} \| \| r_{out})$	Low	High
Common-drain	≈1	High	Low

Appendix B

Published Paper

A 2.3dB NF CMOS Low Voltage LNA Optimized for Medical Applications at 600MHz

A 2.3-dB NF CMOS Low Voltage LNA Optimized for Medical Applications at 600MHz

Rui Borrego, João P. Oliveira, João Goes
CTS-UNINOVA, Departamento de Engenharia Eletrotécnica e Computadores
Faculdade de Ciências e Tecnologia
Universidade Nova de Lisboa
FCT Campus,2857-517 Caparica, Portugal
E-mail: rmb18677@campus.fct.unl.pt, jpao@fct.unl.pt, jg@uninova.pt

Abstract—**In this paper it is presented a balun LNA, with voltage gain control that combines a common-gate and common-source stage, in which transistors biased in triode region replace the resistive loads. This last approach in conjunction with a dynamic threshold reduction technique allows a low supply voltage operation. Furthermore, a significant chip area reduction can be exploited by adopting an inductor-less configuration. Simulations results with a 130 nm CMOS technology show that the gain is up to 19.3 dB and the NF is below 2.3 dB. The total dissipation is 4 mW, leading to an FOM of 2.26 for 0.6 V supply.**

Index Terms—**DTMOS; balun; low voltage; low power**

I. Introduction

The present project for wireless communications includes Industrial, Scientific, and Medical (ISM) and wireless Medical Telemetry Service (WMTS) application [1]. These require low power, low voltage transceivers, which can be fully integrated in a single chip [2, 3], to reduce the area and the cost. A fundamental block in this kind of systems is the Low Noise Amplifier (LNA), which is analyzed in this work.

In this paper, the main goal is to design a low area and low cost LNA, capable to operate at 0.6 V supply voltage with good gain (G) and low noise figure (NF) which can be used in a fall detection microsystem for elder and disable.

Equations for G and NF are presented, which can be used to optimize the circuit performance. Circuit prototypes in 130nm standard CMOS technology at 1.2 V to 0.6 V have been designed and simulated to demonstrate the proposed technique. The circuit prototype at 0.6 V has a gain of 17 dB and NF below 2.3 dB, dissipating only 4 mW, leading to a FOM of 2.26 mW^{-1} is which a high value.

In section II it is described the Low Voltage and Wideband Techniques for LNA. In section III it is presented the proposed circuit to increase gain and reduce NF. In section IV it is presented the simulations results. Finally in section V it is described the conclusions.

This work was supported by national funds through FCT – Portuguese Foundation for Science and Technology under projects PEst-OE/EEI/UI0066/2011 and IMPACT (PTDC/EEA-ELC/101421/2008).

II. Low Voltage and Wideband Techniques for a LNA

A. DTMOS technique

The Dynamic Threshold voltage MOS (DTMOS) technique was firstly introduced in 1994, [8], with the objective to better adapt the transistor operation to a lower power supply. The DTMOS technique is mostly used in digital applications in which the gate and the body of the MOSFET are tied together, as shown in Fig 1. In this case, the threshold voltage V_{Th} is higher at V_{GS}=0 but reduces when the device turns on, thus facilitating the inversion layer formation near the interface between the oxide and the bulk substrate.

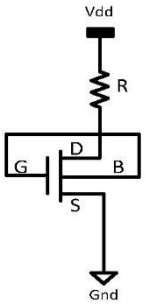


Figure 1. Dynamic threshold MOS (DTMOS).

The threshold voltage of the device in DTMOS configuration is given by

$$V_{Th} = V_{TO} - \gamma * \left(\sqrt{\phi_0} - \sqrt{\phi_0 - V_{BS}}\right) = \\ = V_{TO} - \gamma * \left(\sqrt{\phi_0} - \sqrt{\phi_0 - V_{GS}}\right) \quad (1)$$

where, V_{T0} is the value of V_{Th} for V_{GS}=0, γ is the body-effect coefficient for a given technology, ϕ_0=2 ϕ_F + $\Delta\phi$ (ϕ_F is the Fermi-potential and $\Delta\phi$ is given by 6kT/q ≈ 150 mV at room temperature). Equation (1) clearly shows that the increase of the gate voltage decreases the threshold voltage (V_{Th}), which can be used to improve the level of inversion under low voltage power supply conditions. Not only an higher current can be achieved but also an improvement in its transconductance, g_m , which is given by

$$g_m = \mu C'_{ox} \frac{W}{L} (V_{GS} - V_{Th}) \quad (2)$$

in saturation (C'_{ox} is the oxide gate capacitance per unit area, W and L are the transistor dimensions and μ is the charge mobility). In addition, the bulk related transconductance, g_{mb}, also contributes to improve the overall device gain.

Figure 2 shows an example of the V_{Th} variation with respect to the bulk source V_{BS} voltage for a 130 nm MOS device.

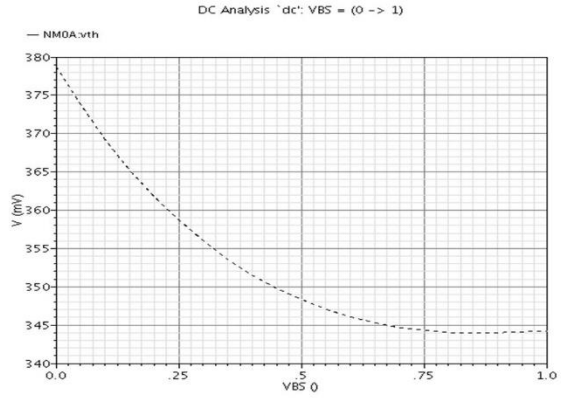


Figure 2. Variation of V_{th} with respect to V_{BS}.

B. Wideband configuration for the I/V load at LNA output

In a traditional LNA, the typical I/V conversion implemented at the output mode is usually based on a LC tank, which contributes for a narrowband frequency response. However, a simple resistor, widening the frequency response of the amplifier, can obtain this I/V operation. One of the problems associated with this approach, under low voltage supply constraints, is the DC voltage drop at the resistor, which can be incompatible with the available total voltage headroom. To overcome this issue, a transistor in triode region can replace the passive resistor, as shown in Fig. 3, since it can reach a similar incremental small signal resistance but with a smaller quiescent DC value for V_{DS}. For example, knowing that the transistor drain current is given by

$$I_D = \mu C'_{ox} \frac{W}{L} \left[(V_{GS} - V_{Th}) V_{DS} - \frac{1}{2} {V_{DS}}^2 \right] \quad (3)$$

in triode region, a value of 1 mA can be achieved with a V_{DS} as low as 150 mV, considering an 130 nm NMOS device with V_{Th}= 0.38 V, $\mu C'_{ox}W/L$ = 5.25 mAV^{-2} and biased with V_{GS} of 0.6 V. The corresponding small signal resistance r_{ds}, at this quiescent point is approximately 370 Ω. If a passive resistor of this value is used instead, the new DC drop voltage increase significantly to 0.37 V, which can be a major concern for low voltage operation.

An additional advantage of using transistors in triode is the gain tuning capability that can be implemented by connecting a controlling voltage the bulk or the gate, as shown in Fig. 3. On the major drawback of this approach is the distortion introduced the device operating in triode. However, not only the signal amplitudes for the LNA are expected to be small, but also the adoption of a differential structure contributes effectively to reduce the even order distortion effects.

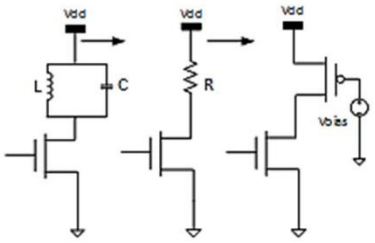


Figure 3. Transistor in triode region with gain tuning.

C. Combined CG and CS used as a Wideband Cancellation Technique

Widening the band of the LNA tends to increase significantly the total input referred noise, since the narrowband filtering has been removed. A possible solution is the balun LNA shown in Fig. 4, [4], in which the thermal noise of M_1 is cancelled out. In fact, the noise produced by M_1 appears in phase at the two output terminals, while the amplified signals that appear at these terminals are in opposition. Therefore, the gain is doubled and the noise is cancelled. It can be shown, [4], that the distortion introduced by M_1 is also reduced (but not totally cancelled).

The differential voltage gain of the LNA is obtained from the gain of a common-gate (CG) stage plus the gain of the common-source (CS) stage:

$$A_v = g_{m1} Rd1 + g_{m2} Rd2 \, . \quad (4)$$

As shown in Fig. 4, the gain of the two stages should be equal for balanced balun operation and for noise cancellation. The maximum gain is limited by the value of the resistors since the input matching sets g_{m1}.

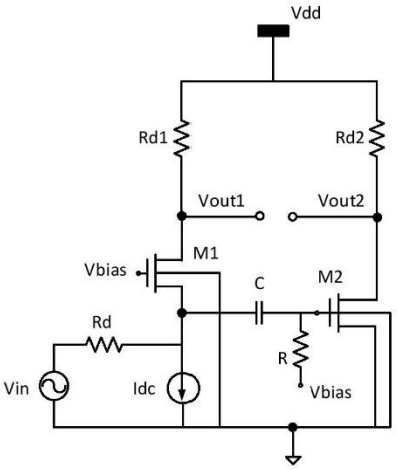


Figure 4. Balun LNA with noise cancellation [4].

III. Proposed LNA with Noise Cancelation and DTMOS Devices

The circuit in the Fig. 4 cannot operate at 0.6 V with good gain and it is limited, therefore it is proposed a solution to solve this limitation. It is replaced resistor load by transistors in triode region and it is used DTMOS in M1, 2, 3, 4 as it is possible so see in the next figure.

In the proposed LNA showed in Fig. 5, a $vbias_{1,\,2,\,3}$ and DTMOS are used to reduce the noise factor, boost the gain and to be possible to make this circuit work between 0.6 V - 1.2 V. The buffer was used to make the conversion from differential to single ended.

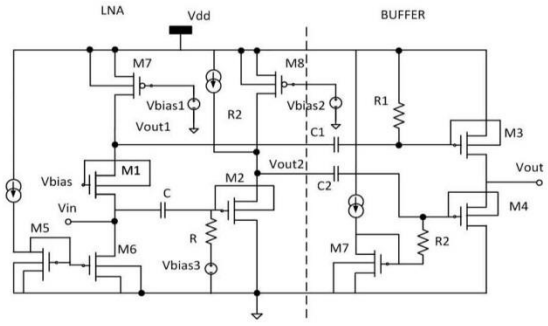


Figure 5. Proposed LNA.

The gain of the proposed LNA as active load is given by:

$$A_v = g_{m1}(r_{d1}//r_{07}) + g_{m1}(r_{d2}//r_{08})\,. \tag{6}$$

The input impedance is given by:

$$Zin = \frac{1}{g_{m1}+g_{m1b}}\quad . \tag{7}$$

From [4, 5] if it is assumed that $g_{m1} = g_{m2} = g_m$ the noise factor is expressed by:

$$F_{LNA} = 1 + \frac{k_f}{8kTR_S coxf^{\alpha f}}\left(\frac{1}{W_1L_1}+\frac{1}{W_2L_2}\right) + \frac{\gamma}{2R_S gm} + \frac{1}{R_S ropgm^2}\,. \tag{8}$$

where k is Boltzman's constant, cox is the oxide gate capacitance per unite area, Wi and Li are the transistor dimensions , T is the absolute temperature, γ is the excess noise factor, kf and αf are intrinsic process parameters, which depend on the size of the transistors [6, 7] .

IV. Design and Simulation Results

Two circuits are optimized using a 130nm CMOS Standard technology, the first one with 1.2 V, the second with 0.6 V.

In the LNA prototype with 1.2 V supply, the transistors have W1=288 um, W2=1296 µm, W3=W4=144 µm, W7=76.8 µm, W8=108 µm. For maximum speed, all transistors have the minimum channel length (120 nm) except M7 which has 240 nm.

For the LNA prototype with 0.6 V supply, the transistors have W1=288 µm, W2=1620 µm, W3=W4=144 µm, W7=76.8 µm, W8=64.8 µm. For maximum speed, all transistors have the minimum channel length (120 nm) except M7 which has 240 nm.

TABLE I. Circuit simulations for 1.2 supply

	BW (GHz)	Av (dB)	NF (dB)	IIP2 (dbm)	IIP3 (dBm)	PDC (mW)	FOM (mW^{-1})
Balun LNA	0.4-0.9	10.5	<3.3	15.3	-3.9	9.5	0.32
Proposed LNA	0.4-0.9	19.3	<2.3	-12.2	-11.2	11.8	1.15

It is seen in the table I with this configuration that, it is obtained a boosting of 9 dB for the gain and is reduced the noise factor in 1 dB approximately, and thus it was obtained also a better figure of merit. On the other hand the IIP2 and IIP3 worsened, but in general are reasonable values.

For comparison the following figure merit is used [8]:

$$FOM[mW^{-1}] = \frac{Gain}{(NF-1)P_{DC}[mW]}\,. \tag{10}$$

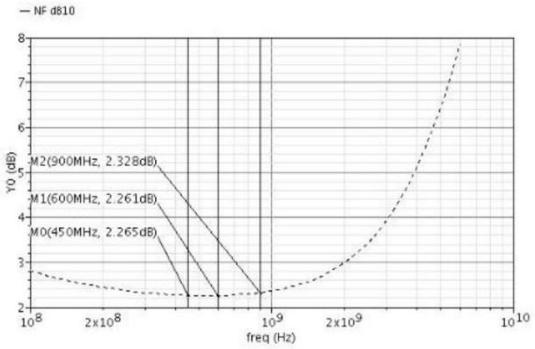


Figure 6. NF simulations for the prototype at 1.2 V.

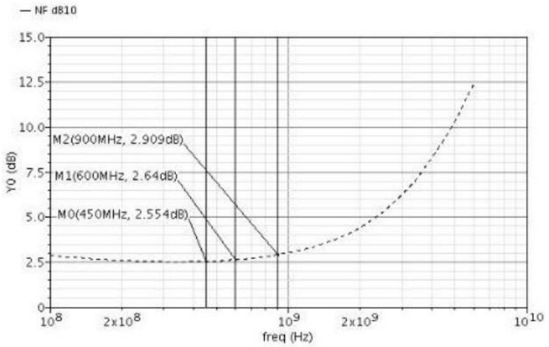


Figure 7. NF simulations for the prototype at 0.6 V.

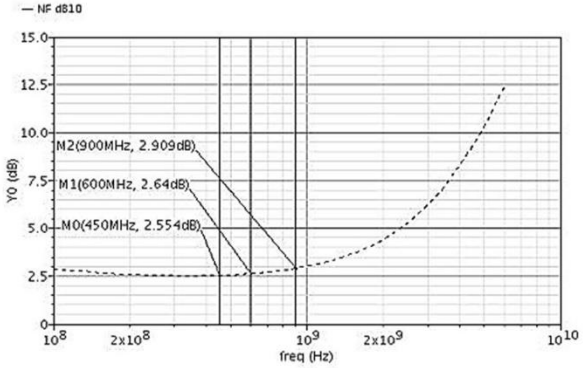


Figure 7. NF simulations for the prototype at 0.6 V.

The noise simulations shown in Fig. 6 and Fig. 7 indicates a slightly degradation of the NF level when the circuit operates at 0.6 V.

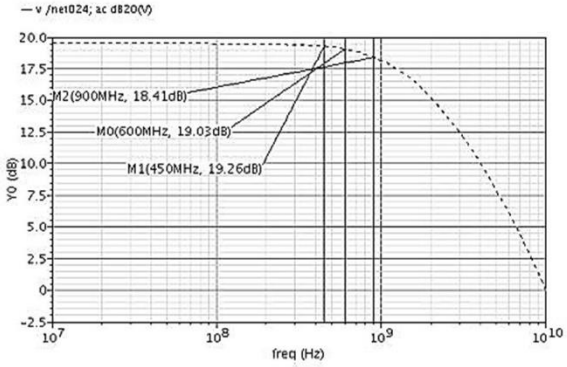


Figure 8. Gain simulation for the prototype with 1.2 V.

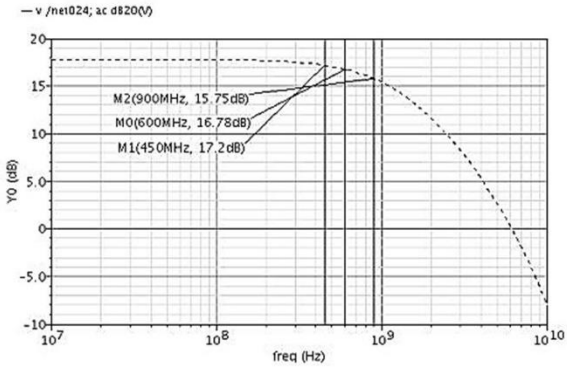


Figure 9. Gain simulation for the prototype at 0.6 V.

A similar conclusion from Figs. 8 and 9, can be made with respect to the slightly lower gain that the LNA achieves when operating at 0.6 V.

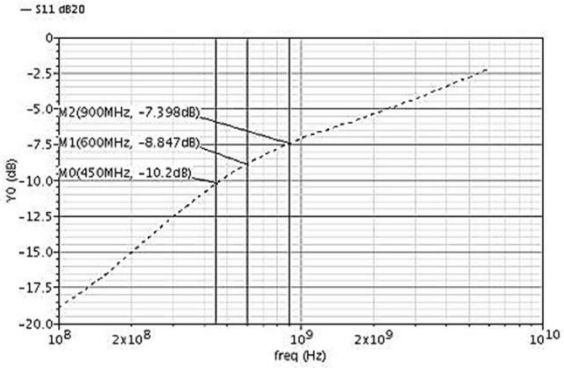


Figure 10. S_{11} parameter simulations for the prototype at 1.2 V.

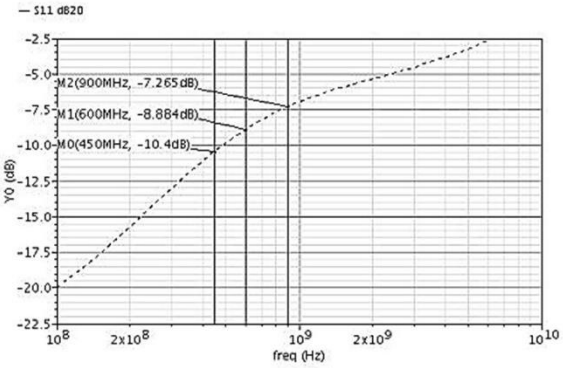


Figure 11. S_{11} parameter simulation for the prototype at 0.6 V.

It is shown through Fig. 10 and Fig. 11 that the value of parameter S_{11} does not change significantly, meaning that the M_1 is maintaining a reasonable matching around -10 dB.

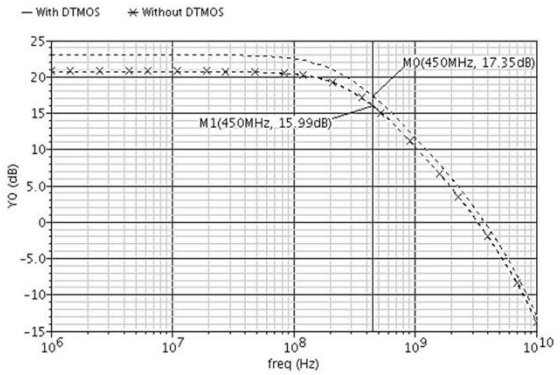


Figure 12. Comparison with and without DTMOS at 0.6 V.

It is also important to make a reference to simulations that show the performance improvements when using DTMOS

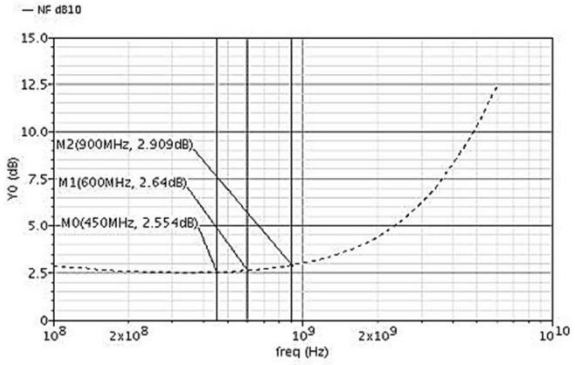


Figure 7. NF simulations for the prototype at 0.6 V.

The noise simulations shown in Fig. 6 and Fig. 7 indicates a slightly degradation of the NF level when the circuit operates at 0.6 V.

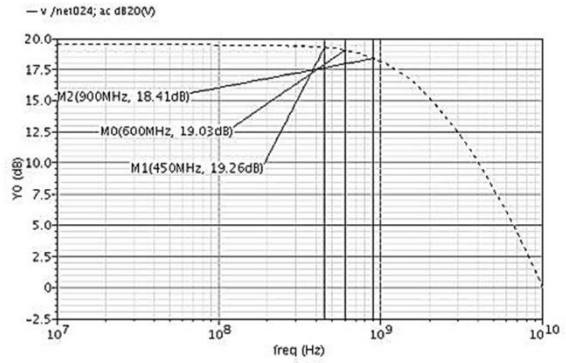


Figure 8. Gain simulation for the prototype with 1.2 V.

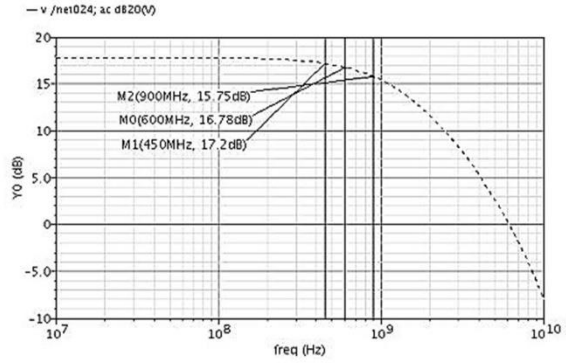


Figure 9. Gain simulation for the prototype at 0.6 V.

A similar conclusion from Figs. 8 and 9, can be made with respect to the slightly lower gain that the LNA achieves when operating at 0.6 V.

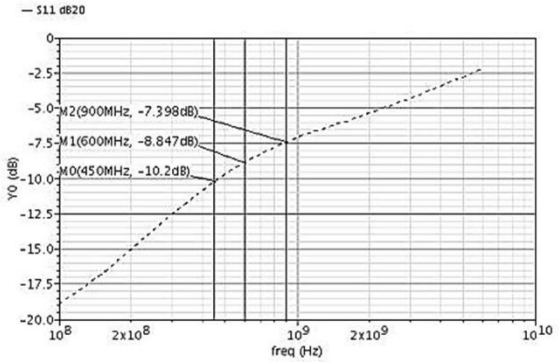


Figure 10. S_{11} parameter simulations for the prototype at 1.2 V.

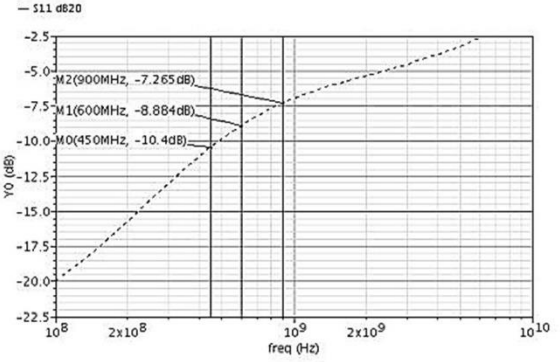


Figure 11. S_{11} parameter simulation for the prototype at 0.6 V.

It is shown through Fig. 10 and Fig. 11 that the value of parameter S_{11} does not change significantly, meaning that the M_1 is maintaining a reasonable matching around -10 dB.

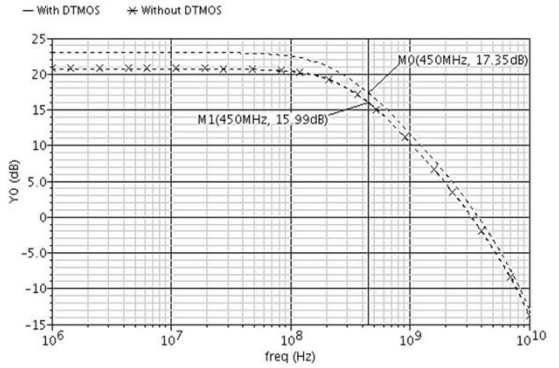


Figure 12. Comparison with and without DTMOS at 0.6 V.

It is also important to make a reference to simulations that show the performance improvements when using DTMOS

configuration on certain transistors. The result shown in Fig. 12 demonstrates that by using DTMOS, an improvement of more than 1.5 dB for the gain and 0.2 dB for NF is possible.

Several PVT simulations were done considering 3 distinct temperatures cases. The obtained results are shown in Figs. 13, 14 and 15.

It is possible to note that, this circuit in general is capable to work in a range of temperatures between 0 and 85° for the three process cases.

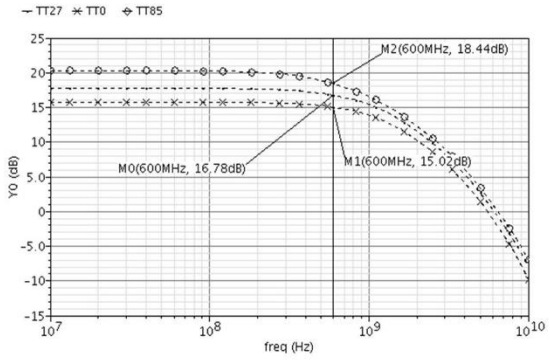


Figure 13. PVT simulation: TT case for the transistors.

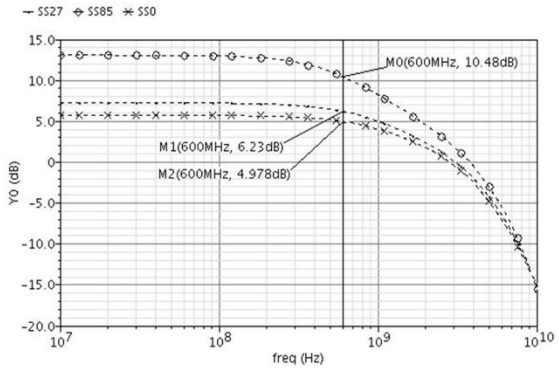


Figure 14. PVT simulation: SS case for the transistors.

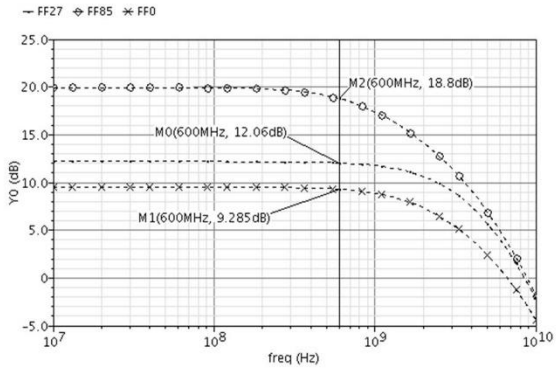


Figure 15. PVT simulation: FF case for the transistors.

Finally, in Table II a comparison with other designs is made.

TABLE II. COMPARISON WITH OTHER LNAS DESIGNS

	Tech (nm)	Band (GHz)	Av (dB)	NF (dB)	PDC (mW)	FOM (mW^{-1})
This work at 1.2 V	130	0.4-0.9	19.3	<2.3	11.8	1.15
This work at 0.6 V	130	0.4-0.9	17.2	<2.6	4	2.14
[10]*	180	0.1-0.9	15	<4.2	10	0.3
[11]*	180	0.5-0.9	16	<4.3	22	0.2

*Values obtained experimentally

V. CONCLUSION

In this paper we present a low power and low voltage LNA capable to work between 0.6 and 1.2 V with high gain and low NF, in 130 nm CMOS technology. Simulation results show that the gain of the LNA, operating at 1.2 V is enhanced to 19.3 dB and at 0.6 V is enhanced to 17.2 dB and the NF is below 2.3 dB for a power consumption of 4 mW operating at 0.6 V. The proposed circuit targets low power and low voltage operation in biomedical applications (ISM and WMTS).

REFERENCES

[1] K. Iniewki, "VLSI Circuits for Biomedical Applications," Artech House 2008.

[2] B. Razavi, RF Microelectronics, Prentice-Hall, 1998.

[3] J. Crols and M. Steyaert, CMOS Wireless Transceiver Design, Kluwer, 1997.

[4] S. Blaakmeer, E. Klumperink, D. Leenaerts, and B. Nauta, "Wideband Balun-LNA with Simultaneous Outputs Balancing, Noise-Canceling and Distortion-Canceling", *IEEE J. Solid-State Circuits*, vol. 43, no. 6,pp. 1341-1350, June 2008.

[5] K.W. Chew, K.S. Yeo, and S. F. Chu, "Effect of technology scaling on the 1/*f* noise of deep submicron MOS transistors", *Solid-State Electron*, vol. 48, pp. 1101-1109, 2004.

[6] M. Manghisoni, L. Ratti, V. Re, V. Speziali, and G. Traversi, "Noise Characterization of 130 nm and 90 nm CMOS Technologies for Analog Front-end Electronics", *IEEE Nuclear Science Symposium Conference*,vol.1, pp. 214 – 218, 2006.

[7] D. Linten, et al, "Low-power 5 GHz LNA and VCO in 90 nm RF CMOS", *2004 Symposium on VLSI Circuits, Digest of TechnicalPapers*, pp. 372 – 375, June 2004.

[8] Fariborz Assederaghi, Member, IEEE, Dennis Sinitsky, Septhen A. Parke, Jeffrey Bokor, Ping K. Ko, Fellow, IEEE, and Chenming Hu, Fellow, IEEE , "Dynamic Threshold- Voltage MOSFET (DTMOS) for Ultra- Low Voltage VLSI" Electron. Lett, vol 38, no. 22,pp. 1362-1364, Oct. 2002.

[9] I. Bastos, L.B. Oliveira, J. Goes, M. Silva, "Balun LNA with continuously controllable gain and with noise and distortion cancellation" *IEEE Int. Symposium Circuit and Systems (ISCAS 2012)*, pp. 2143 - 2146, May 2012.

[10] K. Han; L. Zou; Y. Liao; H. Min; Z. Tang; , "A wideband CMOS variable gain low noise amplifier based on single-to-differential stage for TV tuner applications," *IEEE Solid-State Circuits Conference, A-SSCC '08*, pp.457-460, 3-5 Nov. 2008.

[11] J. Xiao, I. Mehr, J. Silva-Martinez, "A High Dynamic Range CMOS Variable Gain Amplifier for Mobile DTV Tuner," *IEEE J. Solid-State Circuits*, vol.42, no.2, pp.292-301, Feb. 2007.